This document explains the bus timing with the RDY signal. Figure 1 shows an Example of Controlling the Bus Timing with the RDY Signal. “One cycle” here indicates one cycle of BCLK.

When a low signal is input to the RDY pin at the last falling edge of BCLK in the bus cycle, a one-cycle wait is inserted (a change of the bus control signal is delayed for one cycle). After a low signal is detected at the RDY pin, the input signal of the RDY pin is checked at every falling edge of BCLK. When an input signal to the RDY pin is low, a one-cycle wait is inserted; when an input signal is high, a wait is not inserted.

Both high and low inputs to the RDY pin must meet t_{su(RDY-BCLK)} and t_{h(BCLK-RDY)}.

Figure 1  Example of Controlling the Bus Timing with the RDY Signal