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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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M16C/65 Group
Procedure for successive serial I/O transmission/reception using the DMAC

1. Abstract
This application note presents the procedure for successive serial I/O transmission/reception using the DMAC and an example on how to use it.

2. Introduction
This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. **Explanation of the example procedure**

The example procedure selects serial I/O transmission (or reception) for the cause of request to the DMAC, and writes the next data to the transmit buffer (or reads from the receive buffer) at high speed in synchronism with the I/O transmission (or reception). This operation is performed successively as many times as the number of DMAC transfers needed.

3.1 **Example connection**

Figure 1 shows an example device connection for successive transmission/reception.

![Figure 1. Example Connection for Successive Transmission/Reception](image-url)
3.2 Setting-up successive transmission

The following shows how to set up the device for the case where 8 bytes of data are successively transmitted.

Usage Example:

- System
  VCC1=VCC2=5.0V, XIN=16MHz
- DMAC Setting
  DMA Request Factors=UART0 transfer, Single transfer, Transfer unit = 8 bits, Transfer source address direction=Forward direction, Transfer destination address direction=fixed (U0TB register)
- Serial I/O Setting
  Clock synchronous serial I/O mode, BRG count source = f1SIO, Bit Rates=62500bps (BRG=127), Transmit Interrupt Cause=Transmit buffer empty

Operation:

Specify UART0 transmission for the cause of request to the DMAC and after writing the first byte to the UART0 transmit buffer, transmit the remaining 7 bytes of data successively using a UART0 transmit interrupt request as a trigger. Figure 2 shows successive transmission/reception timing.

<table>
<thead>
<tr>
<th>CLK0</th>
<th>TxD0</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Figure 2. Successive Transmission/reception Timing" /></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2. Successive Transmission/reception Timing**
(1) Setting the serial I/O

### Setting UART0 transmit/receive mode register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

UART0 transmit/receive mode register [Address 0248h] U0MR

- **Serial I/O mode select bit**
  - 0 0 1: Clock synchronous serial I/O mode
- **Internal/external clock select bit**
  - 0: Internal clock
- **TXD, RXD I/O polarity reverse bit**
  - 0: No reverse

### Setting UART0 transmit/receive control register 0

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

UART0 transmit/receive control register [Address 024Ch] U0C0

- **U0BRG count source select bit**
  - 0 0: fSiO is selected
- **Transmit register empty flag**
  - 0: Data present in transmit register (during transmission)
  - 1: No data present in transmit register (transmission completed)
- **CTS/RTS disable bit**
  - 1: CTS/RTS function disabled
- **Data output select bit**
  - 0: CMOS output
- **CLK polarity select bit**
  - 0: Transmit data is output at falling edge of transfer clock
- **Transfer format select bit**
  - 0: LSB first

### Setting UART0 transmit/receive control register 1

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

UART0 transmit/receive control register 1 [Address 024Dh] U0C1

- **Transmit enable bit**
  - 0: Transmission disabled
- **Transmit buffer empty bit**
  - 0: Data present in U0TB register
  - 1: No data present in U0TB register
- **Receive enable bit**
  - 0: Reception disabled
- **Receive complete flag**
  - 0: No data present in U0RB register
  - 1: Data present in U0RB register
- **Data logic select bit**
  - 0: No reverse
- **Error signal output enable bit**
  - 0: Output disabled
### Setting UART transmit/receive control register 2

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **UART0 transmit interrupt cause select bit**
  - 0 : Transmit buffer empty
- **UART1 transmit interrupt cause select bit**
- **UART0 continuous receive mode enable bit**
  - 0 : Continuous receive mode disabled
- **UART1 continuous receive mode enable bit**
- **UART1 CLK, CLKS select bit 0**
- **UART1 CLK, CLKS select bit 1**
- **Separate UART0 CTS/RTS bit**
  - 0 : CTS/RTS shared pin

Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to “00h”.

### Setting UART0 bit rate register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
</tr>
</thead>
<tbody>
<tr>
<td>127</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

When the BRG count source = fSIO and f(XIN) = 16MHz, the transfer rate is \((16 \times 10^6) / 2 (127 + 1) = 62,500\) bps

### Setting UART0 transmit interrupt control register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Interrupt priority level select bit**
  - b2 b1 b0
  - 0 0 0 : Level 0 (interrupt disabled)

### (2) Setting the DMAC

### Setting DMA0 source select register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **DMA request source select bit**
  - b4 b3 b2 b1 b0
  - 0 1 0 1 0 : UART0 transmit
- **DMA request source expansion select bit**
  - 0 : Basic request source
### Setting DMA0 control register

DMA0 control register [Address 018Ch] DM0CON

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

- **Transfer unit bit select bit**: 1 : 8 bits
- **Repeat transfer mode select bit**: 0 : Single transfer
- **DMA request bit**: 0 : DMA not requested
- **DMA enable bit**: 0 : Disabled
- **Source address direction select bit**: 1 : Forward (Bit 4 and bit 5 cannot be set to “1” simultaneously)
- **Destination address direction select bit**: 0 : Fixed (Bit 4 and bit 5 cannot be set to “1” simultaneously)

### Setting DMA0 source pointer

DMA0 source pointer [Address 0182h to 0180h] SAR0

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Set the source address of transfer

### Setting DMA0 destination pointer

DMA0 destination pointer [Address 0186h to 0184h] DAR0

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Set the destination address (U0TB) of transfer

### Setting DMA0 transfer counter

DMA0 transfer counter [Address 0189h to 0188h] TCR0

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

Since the first byte of 8-byte successive transmission is written and then transferred to the U0TB register directly (not transferred by the DMAC), set the value “6” here so that 7 bytes will be transferred by DMA.

### Setting DMA0 interrupt control register

DMA0 interrupt control register [Address 004Bh] DM0IC

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Interrupt priority level select bit**: Set the priority level
(3) Enables interrupt (I flag = “1”)

(4) Setting DMA0 control register back again (to enable DMA)

Setting DMA0 control register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DMA0 control register [Address 018Ch] DM0CON

DMA enable bit
1 : Enabled

(5) Enables transmit

Setting the TE bit in the U0C1 register to “1” (transmit enable)

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

UART0 transmit/receive control register 1 [Address 024Dh] U0C1

Transmit enable bit
1 : Transmission enabled

(6) Starting successive transmissions

Write the first byte of successive transmit data to the U0TB register. Thereafter, the other bytes of data are successively transmitted by means of the DMAC transfer initiated by a UART0 transmit interrupt request until the count set in the DMA transfer counter expires.

(7) DMAC transfer complete interrupt processing

Set the DMAC transfer complete flag.
3.3 Setting-up successive reception

The following shows how to set up the device for the case where 8 bytes of data are successively received.

Usage Example:

- **System**
  - VCC1=VCC2=5.0V, XIN=16MHz
- **DMAC Setting**
  - DMA Request Factors=UART0 reception, Single transfer, Transfer unit = 16 bits (including an error flag), Transfer source address direction=fixed (U0RB register), Transfer destination address direction=Forward direction
- **Serial I/O Setting**
  - Clock synchronous serial I/O mode, External clock (Note), Continuous receive mode enabled

Note:

When the input at the CLK0 pin before data reception is high (or low if the CKPOL bit in the U0C0 register = 1), the conditions described below must be met:

- TE bit in the U0C1 register = 1 (transmission enabled)
- RE bit in the U0C1 register = 1 (reception enabled)
- U0RB register is read

Operation:

Specify UART0 reception for the cause of request to the DMAC and after a dummy read of the UART0 receive buffer, receive the data successively using a UART0 receive interrupt as a trigger. Figure 3 shows successive reception timing.

![Figure 3. Successive Reception Timing](image-url)
(1) Setting the serial I/O

**Setting UART0 transmit/receive mode register**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

UART0 transmit/receive mode register [Address 0248h] U0MR

- Serial I/O mode select bit
  - b2 b1 b0: 0 0 1 : Clock synchronous serial I/O mode
  - 1 : External clock

- Internal/external clock select bit
  - 1 : External clock

- TxD, RxD I/O polarity reverse bit
  - 0 : No reverse

**Setting UART0 transmit/receive control register 0**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

UART0 transmit/receive control register [Address 024Ch] U0C0

- Transmit register empty flag
  - 0 : Data present in transmit register (during transmission)
  - 1 : No data present in transmit register (transmission completed)

- CTS/RTS disable bit
  - 1 : CTS/RTS function disabled

- Data output select bit
  - 0 : CMOS output

- CLK polarity select bit
  - 0 : Receive data is input at rising edge

- Transfer format select bit
  - 0 : LSB first

**Setting UART0 transmit/receive control register 1**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

UART0 transmit/receive control register 1 [Address 024Dh] U0C1

- Transmit enable bit
  - 0 : Transmission disabled

- Transmit buffer empty bit
  - 0 : Data present in U0TB register
  - 1 : No data present in U0TB register

- Receive enable bit
  - 0 : Reception disabled

- Receive complete flag
  - 0 : No data present in U0RB register
  - 1 : Data present in U0RB register

- Data logic select bit
  - 0 : No reverse

- Error signal output enable bit
  - 0 : Output disabled
Procedure for successive serial I/O transmission/reception using the DMAC

Setting UART transmit/receive control register 2

```
0 0 1 0
```

- UART0 transmit interrupt cause select bit
  - 0: Transmit buffer empty
- UART1 transmit interrupt cause select bit
- UART0 continuous receive mode enable bit
  - 1: Continuous receive mode enabled
- UART1 continuous receive mode enable bit
- UART1 CLK, CLKS select bit 0
- UART1 CLK, CLKS select bit 1
- Separate UART0 CTS/RTS bit
  - 0: CTS/RTS shared pin

Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to “00h”.

Setting UART0 transmit interrupt control register

```
0 0 0 0 0 0 0 0
```

- Interrupt priority level select bit
  - b2 b1 b0
  - 0 0 0: Level 0 (interrupt disabled)

(2) Setting the DMAC

Setting DMA0 source select register

```
0 0 0 1 0 1 1
```

- DMA request source select bit
  - b4 b3 b2 b1 b0
  - 0 1 0 1 1: UART0 receive
- DMA request source expansion select bit
  - 0: Basic request source
Setting DMA0 control register

DMA0 control register [Address 018Ch] DM0CON

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7, b0</td>
<td>Transfer unit bit select bit</td>
</tr>
<tr>
<td></td>
<td>0: 16 bits</td>
</tr>
<tr>
<td>b5</td>
<td>Repeat transfer mode select bit</td>
</tr>
<tr>
<td></td>
<td>0: Single transfer</td>
</tr>
<tr>
<td>b4</td>
<td>DMA request bit</td>
</tr>
<tr>
<td></td>
<td>0: DMA not requested</td>
</tr>
<tr>
<td>b3</td>
<td>DMA enable bit</td>
</tr>
<tr>
<td></td>
<td>0: Disabled</td>
</tr>
<tr>
<td>b2</td>
<td>Source address direction select bit</td>
</tr>
<tr>
<td></td>
<td>0: Fixed (Bit 4 and bit 5 cannot be set to “1” simultaneously)</td>
</tr>
<tr>
<td>b1, b0</td>
<td>Destination address direction select bit</td>
</tr>
<tr>
<td></td>
<td>1: Forward (Bit 4 and bit 5 cannot be set to “1” simultaneously)</td>
</tr>
</tbody>
</table>

Setting DMA0 source pointer

DMA0 source pointer [Address 0182h to 0180h] SAR0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7, b0</td>
<td>Set the source address (U0RB) of transfer</td>
</tr>
</tbody>
</table>

Setting DMA0 destination pointer

DMA0 destination pointer [Address 0186h to 0184h] DAR0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7, b0</td>
<td>Set the destination address of transfer</td>
</tr>
</tbody>
</table>

Setting DMA0 transfer counter

DMA0 transfer counter [Address 0189h to 0188h] TCR0

Because 8 bytes are to be received, set the transfer count – 1 = 7 here

Setting DMA0 interrupt control register

DMA0 interrupt control register [Address 004Bh] DM0IC

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>Interrupt priority level select bit</td>
</tr>
<tr>
<td></td>
<td>Set the interrupt priority level</td>
</tr>
</tbody>
</table>
(3) Enables interrupt (I flag = “1”)

(4) Setting DMA0 control register back again (to enable DMA)

<table>
<thead>
<tr>
<th>Setting DMA0 control register</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 1 0 0 0</td>
</tr>
<tr>
<td>DMA0 control register [Address 018Ch] DM0CON</td>
</tr>
<tr>
<td>DMA enable bit</td>
</tr>
<tr>
<td>1 : Enabled</td>
</tr>
</tbody>
</table>

(5) Enables transmit/receive

Set the TE and RE bits in the U0C1 register both to “1”, to enable transmission and reception.

<table>
<thead>
<tr>
<th>UART0 transmit/receive control register 1 [Address 024Dh] U0C1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1</td>
</tr>
<tr>
<td>Transmit enable bit</td>
</tr>
<tr>
<td>1 : Transmission enabled</td>
</tr>
<tr>
<td>Receive enable bit</td>
</tr>
<tr>
<td>1 : Reception enabled</td>
</tr>
</tbody>
</table>

(6) Starting successive reception
Access the U0RB register for dummy read to initiate successive reception.

(7) DMAC transfer complete interrupt processing
Check the received data for errors and, if necessary, reinitialize the serial I/O as error processing.
4. Reference

Hardware manual
M16C/65 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
(Use the most recent version of the document on the Renesas Technology Web site.)

Web-site and contact for support

Renesas Technology Web site
http://www.renesas.com/

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http://www.renesas.com/inquiry
csc@renesas.com
## Revision

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Issue date</th>
<th>Revised Page</th>
<th>Point</th>
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<tr>
<td>1.00</td>
<td>2009.10</td>
<td>-</td>
<td>First edition issued</td>
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