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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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M16C/65 Group

Operation of Timer A (timer mode, pulse output function)

1. Abstract

In timer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count source</td>
<td>O Internal count source (f1TIMAB/f2TIMAB/f3TIMAB/f4TIMAB/f6TIMAB/f8TIMAB/f0CO-F/f0CO-S/fc32)</td>
</tr>
<tr>
<td>Pulse output function</td>
<td>No pulse output</td>
</tr>
<tr>
<td>Gate function</td>
<td>O No gate function</td>
</tr>
<tr>
<td></td>
<td>Performs count only for the period in which the TAiIN pin is at “L” level</td>
</tr>
<tr>
<td></td>
<td>Performs count only for the period in which the TAiIN pin is at “H” level</td>
</tr>
<tr>
<td>Output polar control</td>
<td>O Output waveform “H” active</td>
</tr>
<tr>
<td></td>
<td>Output waveform “L” active (output reversed)</td>
</tr>
</tbody>
</table>

Note: i=0~4

4. Operation

(1) Setting the count start flag to “1” causes the counter to perform a down count on the count source.

(2) If an underflow occurs, the content of the reload register is reloaded to the counter, and the count continues. At this time, the timer Ai interrupt request bit goes to “1”. Also, the output polarity of the TAiOUT pin reverses.

(3) Setting the count start flag to “0” causes the counter to stop and to hold its value. Also, the output polarity of the TAiOUT pin outputs an “L” level.

Figure 1 shows the operation timing.
## 5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

### Table 2. Count Source Selection of Timer A

<table>
<thead>
<tr>
<th>TCDIV00</th>
<th>TACSj register (Note 2)</th>
<th>TaMR register</th>
<th>Count source</th>
<th>Count source period</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCDIV00</td>
<td>TCS3</td>
<td>TCS2</td>
<td>TCS1</td>
<td>TCS0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>1</td>
</tr>
</tbody>
</table>

**Note 1:** TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

**Note 2:** TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

**Note 3:** When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.
Figure 2. Count source of Timer A

Selecting a clock used prior to timer AB frequency dividing
(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.)

Timer AB Division Control Register C [Address 01CBh] TCKDIVC0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
</tr>
</tbody>
</table>

Clock select prior to timer AB division bit
0 : f1

Reserved bits
Set to 0

No register bits. If necessary, set to 0. Read as undefined value.

Reserved bits
Set to 0
### Selecting timer count source

TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count source.

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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</tbody>
</table>

Table 2: Timer A count source option specified bit (Note1)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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<tr>
<td>0</td>
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</tbody>
</table>

Note 1: About the count source period, please refer to Table 2.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.
Selecting timer mode and functions

Timer Ai mode register (i=0 to 4)  [Address 0336h to 033Ah] TAiMR (i=0 to 4)

Selection of timer mode
Pulse output function select bit
0 1 : Pulse is output (Note1) (TAiOUT pin is a pulse output pin)
Gate function select bit
0 0 : Gate function not available (TAiIN pin is a normal port pin)
0 (Must always be "0" in timer mode)
Count source select bit (Note2)
0 0 : f1TIMAB or f2TIMAB (Note3)
0 1 : f1TIMAB
1 0 : f2TIMAB
1 1 : f32

Note 1: The settings of the corresponding port register and port direction register are invalid.
Note 2: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.

Selecting waveform output function

Timer A waveform output function select register  [Address 01D5h] TAPOFS
TAOOUT output polar control bit
0 : Output waveform "H" active
TA1OUT output polar control bit
0 : Output waveform "H" active
TA2OUT output polar control bit
0 : Output waveform "H" active
TA3OUT output polar control bit
0 : Output waveform "H" active
TA4OUT output polar control bit
0 : Output waveform "H" active
No register bits. If necessary, set to 0. Read as undefined value

Setting counter value

Timer A0 register  [Address 0327h, 0326h]  TA0
Timer A1 register  [Address 0329h, 0328h]  TA1
Timer A2 register  [Address 032Bh, 032Ah]  TA2
Timer A3 register  [Address 032Dh, 032Ch]  TA3
Timer A4 register  [Address 032Fh, 032Eh]  TA4
Can be set to 0000h to FFFFh
Setting clock prescaler reset flag
(This function is effective when \( f_{\text{C}32} \) is selected as the count source. Reset the prescaler for generating \( f_{\text{C}32} \) by dividing the \( X_{\text{IN}} \) by 32.)

\[
\begin{array}{c}
\text{Address 0015h} \\
\text{CPSRF}
\end{array}
\]

- Count prescaler reset flag
- Clock prescaler reset flag
  - 0 : No effect
  - 1 : Prescale is reset (When read, the value is "0")

Setting count start flag

\[
\begin{array}{c}
\text{Address 0320h} \\
\text{TABSR}
\end{array}
\]

- Count start flag
- Timer A0 count start flag
- Timer A1 count start flag
- Timer A2 count start flag
- Timer A3 count start flag
- Timer A4 count start flag

*Start count*
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Hardware manual
   M16C/65 Group Hardware Manual
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