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April 1st, 2010
Renesas Electronics Corporation

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M16C/65 Group

Operation of Timer A (timer mode, gate function)

1. Abstract

In timer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count source</td>
<td>O Internal count source</td>
</tr>
<tr>
<td></td>
<td>(f1TIMAB/f2TIMAB/f3TIMAB/f4TIMAB/f64TIMAB/foco-F/foco-S/fc32)</td>
</tr>
<tr>
<td>Pulse output function</td>
<td>O No pulse output</td>
</tr>
<tr>
<td></td>
<td>P Pulses output</td>
</tr>
<tr>
<td>Gate function</td>
<td>No gate function</td>
</tr>
<tr>
<td></td>
<td>Performs count only for the period in which the TAiIN pin is at “L” level</td>
</tr>
<tr>
<td></td>
<td>Performs count only for the period in which the TAiIN pin is at “H” level</td>
</tr>
<tr>
<td>Output polar control</td>
<td>O Output waveform “H” active</td>
</tr>
<tr>
<td></td>
<td>P Output waveform “L” active (output reversed)</td>
</tr>
</tbody>
</table>

Note: i=0~4

4. Operation

(1) When the count start flag is set to “1” and the TAiIN pin inputs at “H” level, the counter performs a down count on the count source.

(2) When the TAiIN pin inputs at “L” level, the counter stops and holds its value.

(3) If an underflow occurs, the content of the reload register is reloaded to the counter, and the count continues. At this time, the timer Ai interrupt request bit goes to “1”.

(4) Setting the count start flag to “0” causes the counter to stop and to hold its value.

Note: ▪ Make the pulse width of the signal input to the TAiIN pin not less than two cycles of the count source.

Figure 1 shows the operation timing.
5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

Table 2. Count Source Selection of Timer A

<table>
<thead>
<tr>
<th>TCDIV00 register (Note 1)</th>
<th>TACSj register (Note 2)</th>
<th>TAiMR register</th>
<th>Count source</th>
<th>Count source period</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCS3/ TCS7</td>
<td>TCS2/ TCS6</td>
<td>TCS1/ TCS5</td>
<td>TCS0/ TCS4</td>
<td>TCK1</td>
</tr>
<tr>
<td>0 0 0 - - - 0 0</td>
<td>f1TIMAB/ f2TIMAB (Note 3)</td>
<td>50ns/100ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 - - - 0 1</td>
<td>f8TIMAB</td>
<td>400ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 - - - 1 0</td>
<td>f32TIMAB</td>
<td>1600ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 - - - 1 1</td>
<td>fc32</td>
<td>976.56μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 0 0 0 - -</td>
<td>f1TIMAB/ f2TIMAB (Note 3)</td>
<td>50ns/100ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 0 1 0 - -</td>
<td>f8TIMAB</td>
<td>400ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 1 0 - -</td>
<td>f32TIMAB</td>
<td>1600ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 1 1 - -</td>
<td>f64TIMAB</td>
<td>3200ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1 0 0 0 - -</td>
<td>foco-F</td>
<td>about 50ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1 0 1 - -</td>
<td>foco-s</td>
<td>about 8μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1 1 0 - -</td>
<td>fc32</td>
<td>976.56μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 0 0 - -</td>
<td>f1TIMAB/ f2TIMAB (Note 3)</td>
<td>about 50ns/100ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 0 1 - -</td>
<td>f8TIMAB</td>
<td>about 400ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 1 0 - -</td>
<td>f32TIMAB</td>
<td>about 1600ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 1 1 - -</td>
<td>f64TIMAB</td>
<td>about 3200ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.
Figure 2. Count source of Timer A

Selecting a clock used prior to timer AB frequency dividing
(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved bits</td>
</tr>
<tr>
<td>1</td>
<td>Reserved bits</td>
</tr>
</tbody>
</table>

Clock select prior to timer AB division bit
0: f1

Timer AB Division Control Register 0 [Address 01CBh] TCDIV0C0

Reserved bits
Set to 0
No register bits. If necessary, set to 0. Read as undefined value.
Reserved bits
Set to 0
Operation of Timer A (timer mode, gate function)

Selecting timer count source

TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count source.

TAC0: Timer A count source select register 0 [Address 01D0h]
TAC1: Timer A count source select register 1 [Address 01D1h]
TAC2: Timer A count source select register 2 [Address 01D2h]

TAi (i = 0, 1, 2) count source select bit (Note1)
- 0 0 0: f1TIMAB or f2TIMAB (Note2)
- 0 0 1: f3TIMAB
- 0 1 0: f2TIMAB
- 0 1 1: f4TIMSB
- 1 0 0: fcco-f
- 1 0 1: fcco-s
- 1 1 0: fc32
- 1 1 1: Do not set

TAi count source option specified bit (Note1)
- 0: TCK0, TCK1 enabled, TCS0 to TCS2 disabled
- 1: TCS0 to TCS2 enabled

TAj (i = 0, 1, 2) count source select bit (Note1)
- 0 0 0: f1TIMAB or f2TIMAB (Note2)
- 0 0 1: f3TIMAB
- 0 1 0: f2TIMAB
- 0 1 1: f4TIMSB
- 1 0 0: fcco-f
- 1 0 1: fcco-s
- 1 1 0: fc32
- 1 1 1: Do not set

TAj count source option specified bit (Note1)
- 0: TCK0, TCK1 enabled, TCS4 to TCS6 disabled
- 1: TCS4 to TCS6 enabled

TACS0 register; i = 0, j = 1, TACS1 register; i = 2, j = 3
Note 1: About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.

TA4 count source select bit (Note1)
- 0 0 0: f1TIMAB or f2TIMAB (Note2)
- 0 0 1: f3TIMAB
- 0 1 0: f2TIMAB
- 0 1 1: f4TIMSB
- 1 0 0: fcco-f
- 1 0 1: fcco-s
- 1 1 0: fc32
- 1 1 1: Do not set

TA4 count source option specified bit (Note1)
- 0: TCK0, TCK1 enabled, TCS0 to TCS2 disabled
- 1: TCS0 to TCS2 enabled

No register bits. If necessary, set to 0. Read as undefined value.
Note 1: About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.
Selecting timer mode and functions

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
| Timer Ai mode register (i=0 to 4) [Address 0336h to 033Ah] TAiMR (i=0 to 4)
| Selection of timer mode
| Pulse output function select bit
| 0 : Pulse is not output (TAiOUT pin is a normal port pin)
| Gate function select bit
| b4 b3
| 1 1 : Timer counts only when TAiIN pin is held “H” (Note1)
| 0 (Must always be “0” in timer mode)
| Count source select bit (Note2)
| b7 b6
| 0 0 : f1TIMAB or f2TIMAB (Note3)
| 0 1 : f1TIMAB
| 1 0 : f2TIMAB
| 1 1 : fc32

Note 1: Set the corresponding port direction register to “0”.
Note 2: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.

Selecting waveform output function

| Timer A waveform output function select register [Address 01D5h] TAPOFS
| TA0OUT output polar control bit
| 0 : Output waveform “H” active
| TA1OUT output polar control bit
| 0 : Output waveform “H” active
| TA2OUT output polar control bit
| 0 : Output waveform “H” active
| TA3OUT output polar control bit
| 0 : Output waveform “H” active
| TA4OUT output polar control bit
| 0 : Output waveform “H” active

No register bits. If necessary, set to 0. Read as undefined value.

Setting counter value

<table>
<thead>
<tr>
<th>(b15)</th>
<th>(b8)</th>
<th>(b7)</th>
<th>(b0)</th>
</tr>
</thead>
</table>
| Timer A0 register [Address 0327h, 0326h] TA0
| Timer A1 register [Address 0329h, 0328h] TA1
| Timer A2 register [Address 032Bh, 032Ah] TA2
| Timer A3 register [Address 032Dh, 032Ch] TA3
| Timer A4 register [Address 032Fh, 032Eh] TA4

Can be set to 0000h to FFFFh
**Setting clock prescaler reset flag**

(This function is effective when $f_{32}$ is selected as the count source. Reset the prescaler for generating $f_{32}$ by dividing the $X_{CN}$ by 32.)

- **Count prescaler reset flag** [Address 0015h]
  - **CPSRF**

- **Clock prescaler reset flag**
  - **b7**
  - **b0**

  0 : No effect
  1 : Prescale is reset (When read, the value is “0”)

**Setting count start flag**

- **Count start flag** [Address 0320h]
  - **TABSR**

- **Timer A0 count start flag**
- **Timer A1 count start flag**
- **Timer A2 count start flag**
- **Timer A3 count start flag**
- **Timer A4 count start flag**

*Start count*
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<td>-</td>
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