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April 1st, 2010
Renesas Electronics Corporation

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1. Abstract

In pulse width modulation mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count source</td>
<td>O Internal count source (f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/foco-f/foco-s/fc32)</td>
</tr>
<tr>
<td>PWM mode</td>
<td>O 16-bit PWM</td>
</tr>
<tr>
<td></td>
<td>8-bit PWM</td>
</tr>
<tr>
<td>Count start condition</td>
<td>External trigger input (falling edge of input signal to the TAiIN pin)</td>
</tr>
<tr>
<td></td>
<td>O External trigger input (rising edge of input signal to the TAiIN pin)</td>
</tr>
<tr>
<td></td>
<td>Timer overflow (TB2/TAj/TAk overflow)</td>
</tr>
<tr>
<td>Output polar control</td>
<td>O Output waveform “H” active</td>
</tr>
<tr>
<td></td>
<td>Output waveform “L” active (output reversed)</td>
</tr>
</tbody>
</table>

Note: j = i – 1, but j = 4 when i = 0; k = i + 1, but k = 0 when i = 4.

4. Operation

(1) If the TAiIN pin input level changes from “L” to “H” with the count start flag set to “1”, the counter performs a down count on the count source. Also, the TAiOUT pin outputs an “H” level.

(2) The TAiOUT pin output level changes from “H” to “L” when a set time period elapses. At this time, the timer Ai interrupt request bit goes to “1”.

(3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.

(4) Setting the count start flag to “0” causes the counter to stop and to hold its value. Also, the TAiOUT outputs an “L” level.

Note:
The period of PWM pulses becomes \((2^{16} – 1)/fi\), and the “H” level pulse width becomes n/fi. If the timer Ai register is set to “0000h”, the pulse width modulator does not work, and the TAiOUT pin outputs “L” level, therefore the timer Ai interrupt request is not generated.

\((fi : frequency of the count source f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/foco-s/fc32; n : value of the timer)\)

Figure 1 shows the operation timing.
Figure 1. Operation timing of pulse width modulation mode, 16-bit PWM mode
5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

### Table 2. Count Source Selection of Timer A

<table>
<thead>
<tr>
<th>TCDIV00</th>
<th>TACSj register (Note 2)</th>
<th>TAiMR register</th>
<th>Count source</th>
<th>Count source period</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCDIV00</td>
<td>TCS3/ TCS7</td>
<td>TCS2/ TCS6</td>
<td>TCS1/ TCS5</td>
<td>TCK1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.
Selecting a clock used prior to timer AB frequency dividing
(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit,
set other registers associated with timer A again.)

Timer AB Division Control Register C [Address 01CBh]  TCKDIVC0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>C</td>
<td>C</td>
<td>X</td>
<td>C</td>
<td>C</td>
<td>0</td>
<td>C</td>
</tr>
</tbody>
</table>

Clock select prior to timer A8 division bit
0: f1

Reserved bits
Set to 0

No register bits. If necessary, set to 0. Read as undefined value.
Reserved bits
Set to 0

Figure 2. Count source of Timer A
### Selecting timer count source

TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count source.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Example</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>TAi count source select bit (Note1)</td>
<td>TACS0</td>
<td></td>
</tr>
<tr>
<td>b6</td>
<td>TAi count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b5</td>
<td>TAi count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b4</td>
<td>TAi count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b3</td>
<td>TAi count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b2</td>
<td>TAi count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b1</td>
<td>TAi count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b0</td>
<td>TAi count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TACS0 register:** i = 0, j = 1, TACS1 register: i = 2, j = 3

**Note:** About the count source period, please refer to Table 2.

**Note 2:** When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is fTIMAB. When the PCLK0 bit is “0”, the selected clock source is fTIMAB.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Example</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>TAj count source select bit (Note1)</td>
<td>TACS1</td>
<td></td>
</tr>
<tr>
<td>b6</td>
<td>TAj count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b5</td>
<td>TAj count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b4</td>
<td>TAj count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b3</td>
<td>TAj count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b2</td>
<td>TAj count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b1</td>
<td>TAj count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b0</td>
<td>TAj count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TACS0 register:** i = 0, j = 1, TACS1 register: i = 2, j = 3

**Note:** About the count source period, please refer to Table 2.

**Note 2:** When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is fTIMAB. When the PCLK0 bit is “0”, the selected clock source is fTIMAB.

### Timer A count source select register 2 [Address 01D2h] TACS2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Example</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>TA4 count source select bit (Note1)</td>
<td>TACS2</td>
<td></td>
</tr>
<tr>
<td>b6</td>
<td>TA4 count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b5</td>
<td>TA4 count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b4</td>
<td>TA4 count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b3</td>
<td>TA4 count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b2</td>
<td>TA4 count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b1</td>
<td>TA4 count source select bit (Note1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b0</td>
<td>TA4 count source option specified bit (Note1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** About the count source period, please refer to Table 2.

**Note 2:** When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is fTIMAB. When the PCLK0 bit is “0”, the selected clock source is fTIMAB.

No register bits. If necessary, set to 0. Read as undefined value.
Selecting PWM mode and functions

- Timer Ai mode register (i=0 to 4) [Address 0336h to 033Ah]
  - TAiMR (i=0 to 4)
  - Selection of PWM mode
  - External trigger select bit
    - 1: Rising edge of TAin pin's input signal (Note1)
  - Trigger select bit
    - 1: Selected by event/trigger select register
  - 16/8-bit PWM mode select bit
    - 0: Functions as a 16-bit pulse width modulator
    - 1: Functions as an 8-bit pulse width modulator

Count source select bit (Note2)
- b7 b6
  - 0 0: f1TIMAB or f2TIMAB (Note3)
  - 0 1: f1TIMAB
  - 1 0: f2TIMAB
  - 1 1: f32

Note 1: Valid when bits TAiTGH and TAiTGL bit in the ONSF register or TRGSR register are set to 00b (TAin pin input). Please set the port direction bit for the TAiIN pin to 0 (input mode).

Note 2: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.

Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.

Clearing timer Ai interrupt request bit

Refer to 'Precaution for Timer A (pulse width modulation mode)'

- Timer Ai interrupt control register [Address 0055h to 0059h]
  - TAiC (i=0 to 4)
  - Interrupt request bit
Setting event/trigger select bit

- One-shot start flag [Address 0322h] ONSF
- Timer A0 event/trigger select bit
  - b7 b6 0 : Input on TA0n is selected (Note 1)

- Timer A1 event/trigger select bit
  - b1 b0 0 : Input on TA1n is selected (Note 1)

- Timer A2 event/trigger select bit
  - b3 b2 0 : Input on TA2n is selected (Note 1)

- Timer A3 event/trigger select bit
  - b5 b4 0 : Input on TA3n is selected (Note 1)

- Timer A4 event/trigger select bit
  - b7 b6 0 : Input on TA4n is selected (Note 1)

Note 1: Set the port direction bits for the pins TA0n to TA4n to 0 (input mode).

Setting PWM pulse's “H” level width

- Can be set to 0000h to FFFEh

Selecting waveform output function

- Timer A waveform output function select register [Address 01D5h] TAPOFS
  - TA0OUT output polar control bit
    - 0 : Output waveform “H” active
  - TA1OUT output polar control bit
    - 0 : Output waveform “H” active
  - TA2OUT output polar control bit
    - 0 : Output waveform “H” active
  - TA3OUT output polar control bit
    - 0 : Output waveform “H” active
  - TA4OUT output polar control bit
    - 0 : Output waveform “H” active

No register bits. If necessary, set to 0. Read as undefined value.
Operation of Timer A (pulse width modulation mode, 16-bit PWM mode)

**Setting clock prescaler reset flag**
(This function is effective when \( f_{C32} \) is selected as the count source. Reset the prescaler for generating \( f_{C32} \) by dividing the \( X_{cin} \) by 32.)

![Clock prescaler reset flag diagram](image)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Count prescaler reset flag** [Address 0015h]
  - **CPSRF**

| Count prescaler reset flag | 0 : No effect | 1 : Prescaler is reset (When read, the value is “0”) |

**Setting count starts flag**

![Count starts flag diagram](image)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Count start flag** [Address 0320h]
  - **TABS**
  - Timer A0 count start flag
  - Timer A1 count start flag
  - Timer A2 count start flag
  - Timer A3 count start flag
  - Timer A4 count start flag

**Start count**
6. Reference

Hardware manual
M16C/65 Group Hardware Manual
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