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April 1st, 2010
Renesas Electronics Corporation

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M16C/65 Group
Operation of serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

1. Abstract
In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction
This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock prior to division select</td>
<td>f1</td>
<td>Transfer format</td>
<td>LSB first</td>
</tr>
<tr>
<td></td>
<td>foco-F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peripheral clock</td>
<td>f1sio</td>
<td>Transmission interrupt factor</td>
<td>Transmission buffer empty</td>
</tr>
<tr>
<td></td>
<td>f2sio</td>
<td></td>
<td>Transmission complete</td>
</tr>
<tr>
<td>Transfer clock source</td>
<td>Internal clock (f1sio/f2sio/f8sio/f32sio)</td>
<td>Output transfer clock to multiple pins (Note 1)</td>
<td>Not selected</td>
</tr>
<tr>
<td></td>
<td>External clock (CLKi pin)</td>
<td></td>
<td>Selected</td>
</tr>
<tr>
<td>CTS function</td>
<td>CTS function enabled</td>
<td>Serial data logic</td>
<td>No reverse</td>
</tr>
<tr>
<td></td>
<td>CTS function disable</td>
<td></td>
<td>Reverse</td>
</tr>
<tr>
<td>CLK polarity</td>
<td>Output transmission data at the falling edge of the transfer clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output transmission data at the rising edge of the transfer clock</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: This can be selected only when UART1 is used in combination with the internal clock.

4. Operation

(1) Setting the transmit enable bit to “1” makes data transmissible status ready.

(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that the transmission is completed. The transfer clock stops at “H” level. At this time, the UART1 transmit interrupt request bit goes to “1”.

(4) Setting CLK/CLKS select bit 1 to “1” and setting CLK/CLKS select bit 0 to “1” causes the CLKS1 pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.
Figure 1 shows the operation timing.

Example of wiring

Microcomputer

- TxD1 (P6_7)
- CLKS1 (P6_4)
- CLK1 (P6_5)

IN
CLK

IN
CLK

Note: This applies when performing only transmission with an internal clock selected in the clock synchronous serial I/O mode.

Example of operation

1. Transmission enabled
2. Start transmission
3. Transmission is complete
4. Clock switched

Transfer clock
Transmit enable bit (TE)
Transmit buffer empty flag (TI)
CLK, CLKS select bit 1 (CLKMD1)
CLK, CLKS select bit 0 (CLKMD0)
CLK1
CLKS1
TxD1

UART1 Transmit interrupt request bit (RI)

'1'
'0'

Cleared to '0' when interrupt request is accepted, or cleared by software

Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected
5. Set-up procedure

**Setting UART clock select register**

(SET the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)

- UART clock select register [Address 0252h] \( \text{UCLKSEL0} \)
  - Set to “0”
  - UART0 to UART2 clock prior to division select bit
    - 0 : \( f_1 \)
  - UART5 to UART7 clock prior to division select bit
    - 0 : \( f_1 \)

Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

**Setting UART1 transmit/receive mode register**

- UART1 transmit/receive mode register [Address 0258h] \( \text{U1MR} \)
  - Must be fixed to “001”
  - Internal/external clock select bit
    - 0 : Internal clock
  - Invalid in clock synchronous I/O mode
  - Invalid in clock synchronous I/O mode
  - Invalid in clock synchronous I/O mode
  - TxD, RxD I/O polarity reverse bit
    - Usually set to “0”
Setting UART1 transmit/receive control register 0

- **UiBRG count source select bit**
  - b7 b0
  - 00: fSIO or f2SIO is selected (Note1)
  - 01: fSIO is selected
  - 10: f2SIO is selected
  - 11: Do not set to this value

- **CTS/RTS function select bit** (Valid when bit4 = “0”)
  - 0: Data present in transmit register (during transmission)
  - 1: No data present in transmit register (transmission completed)

- **CTS/RTS disable bit**
  - 0: CTS/RTS function disabled
  - 1: CTS/RTS function disabled

- **Data output select bit**
  - 0: Pins TxDi/SDAi and SCLi are CMOS output
  - 1: Pins TxDi/SDAi and SCLi are N-channel open-drain output

- **CLK polarity select bit**
  - 0: Transmission data is output at falling edge of transfer clock and reception data is input at rising edge

- **Transfer format select bit**
  - 0: LSB first

Note 1: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is fSIO. When the PCLK0 bit is “0”, the selected clock source is f2SIO.

Setting UART transmit/receive control register 2

- **UART1 transmit interrupt cause select bit**
  - 0: Transmit buffer empty (TI = 1)

- **CLK/CLKS select bit**
  - 0: Clock output to CLK1
  - 1: Clock output to CLKS1

- **UART1 CLK/CLKS select bit**
  - 0: Transfer clock output from multiple pins function selected

Setting UART1 bit rate register

- **Can be set to 00h to FFh (Note)**

Note: Write to the UiBRG register while serial interface is neither transmitting nor receiving. Use MOV instruction to write to the UiBRG register. Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.
### Transmission enabled

UART1 transmit/receive control register 1 [Address 025Dh]

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Transmit enable bit
1: Transmission enabled

### Writing transmit data

UART1 transmit buffer register [Address 025Bh, 025Ah]

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Setting transmission data

### Start transmission

### Checking the status of UART1 transmit/receive control register

UART1 transmit/receive control register 0 [Address 025Ch]

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Transmit register empty flag
0: Data present in transmit register (during transmission)
1: No data present in transmit register (Writing next transmit data enabled)

### Writing next transmit data

UART1 transmit buffer register [Address 025Bh, 025Ah]

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Setting transmission data

### Transmission is complete
6. Reference

Hardware manual
   M16C/65 Group Hardware Manual
   (Use the most recent version of the document on the Renesas Technology Web site.)

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### Revision

<table>
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<tr>
<th>Rev.</th>
<th>Issue date</th>
<th>Revised Page</th>
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<tbody>
<tr>
<td>1.00</td>
<td>2009.10</td>
<td>-</td>
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