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M16C/65 Group
Operation of DMAC (one-shot transfer mode)

1. Abstract
In one-shot transfer mode, choose functions from the items shown in Table 1. Operations of the circled items are described below.

2. Introduction
This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer space</td>
<td>Fixed address from an arbitrary 1 M bytes space</td>
</tr>
<tr>
<td></td>
<td>Arbitrary 1 M bytes space from a fixed address</td>
</tr>
<tr>
<td></td>
<td>Fixed address from fixed address</td>
</tr>
<tr>
<td>Unit of transfer</td>
<td>O 8 bits</td>
</tr>
<tr>
<td></td>
<td>16 bits</td>
</tr>
<tr>
<td>Repeat transfer mode</td>
<td>O Signal transfer</td>
</tr>
<tr>
<td></td>
<td>Repeat transfer</td>
</tr>
<tr>
<td>Source address direction</td>
<td>O Fixed</td>
</tr>
<tr>
<td></td>
<td>O Forward</td>
</tr>
<tr>
<td>Destination address direction</td>
<td>O Fixed</td>
</tr>
<tr>
<td></td>
<td>O Forward</td>
</tr>
</tbody>
</table>

4. Operation

(1) When software trigger is selected, setting software DMA request bit to “1” generates a DMA transfer request signal.

(2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi forward-direction address pointer are transferred to the address indicated by the DMAi destination pointer. When data transfer starts directly after DMAC becomes active, the value of the DMAi transfer counter reload register is reloaded to the DMAi transfer counter, and the value of the DMAi source pointer is reloaded by the DMAi forward-direction address pointer. Each time a DMA transfer request signal is generated, 1 byte of data is transferred. The DMAi transfer counter is down counted, and the DMAi forward-direction address pointer is up counted.

(3) If the DMA transfer counter underflows, the DMA enable bit changes to “0” and DMA transfer is completed. The DMA interrupt request bit changes to “1” simultaneously.
Figure 1 shows an example of operation of one-shot transfer mode.

<table>
<thead>
<tr>
<th>BCLK</th>
<th>Address bus</th>
<th>RD signal</th>
<th>WR signal</th>
<th>Data bus</th>
<th>Write signal to software DMAi request bit</th>
<th>DMAi request bit</th>
<th>DMA transfer counter</th>
<th>DMAi interrupt request bit</th>
<th>DMAi enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CPU use</td>
<td>Source</td>
<td>Destination</td>
<td>CPU use</td>
<td>Source</td>
<td>CPU use</td>
<td>Indeterminate</td>
<td>0fh</td>
<td>FFh</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- In the case in which the number of transfer times is set to 2.

**Figure 1. Example of operation of one-shot transfer mode**
### 5. Set-up procedure

#### Setting DMAi request cause select register

- **DMA0 request cause select register** [Address 00398h] : DM0SL
- **DMA1 request cause select register** [Address 0039Ah] : DM1SL
- **DMA2 request cause select register** [Address 00399h] : DM2SL
- **DMA3 request cause select register** [Address 00392h] : DM3SL

- DMA request cause select bit
  - b4 b3 b2 b1 b0
  - 0 0 0 0 1 : Software trigger
  - Software DMA request bit
  - Set to "0"

#### Setting DMAi control register

- **DMA0 control register** [Address 0018Ch] : DM0CON
- **DMA1 control register** [Address 0019Ch] : DM1CON
- **DMA2 control register** [Address 001ACh] : DM2CON
- **DMA3 control register** [Address 001BCh] : DM3CON

- Transfer unit bit select bit
  - 1 : 8 bits
- Repeat transfer mode select bit
  - 0 : Signal transfer
- DMA request bit
  - 0 : DMA not requested
- DMA enable bit
  - 0 : Disabled
- Source address direction select bit
  - 1 : Forward (Bit 4 and bit 5 cannot be set to "1" simultaneously)
- Destination address direction select bit
  - 0 : Fixed (Bit 4 and bit 5 cannot be set to "1" simultaneously)

#### Setting DMAi source pointer

- **DMA0 source pointer** [Address 00182h to 00180h] : SAR0
- **DMA1 source pointer** [Address 00192h to 00190h] : SAR1
- **DMA2 source pointer** [Address 001A2h to 001A0h] : SAR2
- **DMA3 source pointer** [Address 001B2h to 001B0h] : SAR3

- Source pointer
  - Stores the source address

#### Setting DMAi destination pointer

- **DMA0 destination pointer** [Address 00186h to 00184h] : DAR0
- **DMA1 destination pointer** [Address 00196h to 00194h] : DAR1
- **DMA2 destination pointer** [Address 001A6h to 001A4h] : DAR2
- **DMA3 destination pointer** [Address 001B6h to 001B4h] : DAR3

- Destination pointer
  - Stores the destination address
Start DMA transmission

Setting DMAi transfer counter

DMA0 transfer counter [Address 0189h to 0188h] TCR0
DMA1 transfer counter [Address 0199h to 0198h] TCR1
DMA2 transfer counter [Address 01A9h to 01A8h] TCR2
DMA3 transfer counter [Address 01B9h to 01B8h] TCR3

Transfer counter
Set a value one less than the transfer count

Setting DMAi control register

DMA0 control register [Address 018Ch] DM0CON
DMA1 control register [Address 019Ch] DM1CON
DMA2 control register [Address 01ACH] DM2CON
DMA3 control register [Address 01BCh] DM3CON

DMA enable bit
1: Enabled

Note: Clear DMA request bit simultaneously again.

When software DMA request bit = “1”
6. Reference

Hardware manual

M16C/65 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
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<th>Rev.</th>
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<th>Revised</th>
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