1. Abstract

This document describes the master transmit/receive processes in I2C-bus interface single master communication using the M16C/63, 64, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M and 57 Groups serial interface (UART2) special mode 1 (I2C mode).

For details on UART2 special mode 1, refer to the M16C Family I2C-bus Interface Using UARTi Special Mode 1 application note.

If this application note is applied for using channels except UART2, see the user's manual, and modify registers related to UARTi.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCUs: M16C/65 Group and M16C/65C Group
- XIN Clock: 20 MHz

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the user’s manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

3.1 Program Outline

Transmission is performed in 3-byte data both in master transmission and reception. Master transmission and reception are repeated alternately. The transmission and reception procedures conform to the I2C-bus communication protocol when used under the following conditions:

- Slave address: 7 bits
- Transfer rate: Approximately 350 kbps (1)
- Transfer data length: 1 to 255 bytes (not including the slave address)
- Single master communication (multi-master is not supported)
- Restart condition generation is not supported

Note:

1. The setting value is 384 kbps.

When the clock synchronous function is enabled, there is a sampling delay of the noise filter width plus 1 to 1.5 cycles of the U2BRG count source. As there is also a delay of the SCL clock when high is determined, the SCL clock high width is extended. Therefore, the actual SCL clock becomes slower than SCL clock transfer rate setting.

In this application example, the actual transfer rate becomes approximately 350 kbps since the clock synchronous function is enabled (reference value: pull up voltage 5 V, pull up resistance 1 kΩ).

Standard-mode and Fast-mode are supported.

Figure 3.1 shows the Communication Format, Figure 3.2 shows the Block Diagram, Figure 3.3 shows the Outline Flowchart, and Figure 3.4 to Figure 3.6 show Timing Diagrams.

![Communication Format Diagram](image-url)

**Figure 3.1 Communication Format**

**Notes:**
- ST: Start condition
- SP: Stop condition
- W: Write is 0
- R: Read is 1
- ACK: Acknowledge is 0
- NACK: Not acknowledge is 1
I2C-bus Interface Using UARTi Special Mode 1
(Master Transmit/Receive)

Figure 3.2  Block Diagram
Figure 3.3 Outline Flowchart

The numbers in Figure 3.3 correspond to the numbers indicated in the program processing in the operating timing charts in Figure 3.4 to Figure 3.6.

1. Initial setting
   Initialize the system clock, UART2 associated SFRs, and variables used.

2. Start master control
   Enable the start/stop condition generation interrupt and generate a start condition.

3. Start/stop condition generation interrupt
   An interrupt request is generated when start condition generation is completed and a stop condition is detected. When start condition generation is completed, the UART2 transmit interrupt is enabled and the slave address is transmitted. When a stop condition is detected, SFR values which changed during communication are returned to their initial values.

4. UART2 transmit interrupt
   A UART2 transmit interrupt is generated at the falling edge of the ninth bit of the SCL clock. When transmitting, set the next byte transmit data. When receiving, set ACK/NACK for the next byte. When communication is completed, generate a stop condition.
Figure 3.4 Master Transmit Timing

- **Start condition**
  - SDA (master output)
  - SCL (master output)
  - Initial setting
  - STPREQ bit in the U2SMR4 register
  - STSPSEL bit in the U2SMR4 register
  - CKPH bit in the U2SMR3 register
  - Program processing
  - UART2 transmit interrupt

- **Stop condition**
  - SDA (slave output)
  - SCL (slave output)
  - Becomes 0 when a start condition is generated.
  - ACK
  - STPREQ bit in the U2SMR4 register
  - STSPSEL bit in the U2SMR4 register
  - CKPH bit in the U2SMR3 register
  - Program processing
  - UART2 transmit interrupt
  - Stop condition detection interrupt
I²C-bus Interface Using UARTi Special Mode 1
(Master Transmit/Receive)

Figure 3.5 Master Receive Timing (1)

Figure 3.6 Master Receive Timing (2)
3.1.1 Peripheral Functions

Serial interface (UART2) special mode 1 (I2C mode) is used under the following setting conditions:

- I2C mode is used.
- Transfer clock is internal clock source.
- $f_1$ is used as U2BRG count source.
- SDA2 and SCL2 pins are N-channel open drain.
- Transfer format uses MSB first.
- Transmission completed (TXEPT = 1) is selected as the UART2 transmit interrupt source.
- Clock delay is used.
- Seven to eight cycles of U2BRG count source is selected as SDA2 digital delay value.
- Clock synchronization is enabled.
- SCL2 wait function is disabled.
- SDA2 output disable function is not used.
- Start/stop condition generation interrupt is used.
- UART2 transmit interrupt is used.
- UART2 receive interrupt is not used.
- Transfer rate is approximately 384 kbps.

Calculating the transfer rate:
Transfer rate $= \frac{U2BRG \text{ count source}}{2 \times (U2BRG \text{ register setting value} + 1)}$

$= \frac{20 \text{ MHz} (f_1)}{2 \times (25 + 1)}$

$\approx 384.615 \text{ kbps}$

Table 3.1 Pins Used and Their Function

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P7_1/SCL2</td>
<td>I/O</td>
<td>I2C mode clock I/O pin</td>
</tr>
<tr>
<td>P7_0/SDA2</td>
<td>I/O</td>
<td>I2C mode data I/O pin</td>
</tr>
</tbody>
</table>

3.1.2 Notes on Using the Attached Sample Program

Note the following when using the program included with this application note:

- Do not use multiple interrupts.
- When setting the system clock to anything other than the XIN clock (20 MHz), change the setting value of the U2BRG count source and the U2BRG register according to the transfer rate calculation shown in 3.1.1 Peripheral Functions.
- If pins SDAi and SCLi are not N-channel open drain, set the NCH bit in the UiC0 register to 1 (pins TXDi/SDAi and SCLi are N-channel open drain output).
- UART0 and UART1 transmit interrupt source select bits exist in the UCON register in M16C/60 Series. Set the U0IRS bit or U1IRS bit in the UCON register to 1 (transmission completed (TXEPT = 1)).
### 3.2 Memory

<table>
<thead>
<tr>
<th>Memory</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>572 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>8 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>Maximum user stack</td>
<td>19 bytes</td>
<td></td>
</tr>
<tr>
<td>Maximum interrupt stack</td>
<td>30 bytes</td>
<td></td>
</tr>
</tbody>
</table>

Usage memory size varies depending on C compiler version and compile options. The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.45 Release 01
- Compile option: `-c -finfo -dir "$(CONFIGDIR)"`
4. Software

This chapter shows the program example to set the example described in chapter 3. Application Example. Refer to the latest hardware user’s manual for details on individual registers.

4.1 Variables

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_tx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Transmit buffer</td>
</tr>
<tr>
<td>unsigned char iic_rx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Receive buffer</td>
</tr>
<tr>
<td>unsigned char retry_counter</td>
<td>1 byte</td>
<td>Count number of communication retries</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>static byte_dt iic_str1</td>
<td>-</td>
<td>Structure to store slave address</td>
</tr>
<tr>
<td>Structure member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>iic_slave_addr</td>
<td>1 byte</td>
<td>Slave address</td>
</tr>
<tr>
<td>iic_rw</td>
<td>b0</td>
<td>R/W flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Write (W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Read (R)</td>
</tr>
<tr>
<td></td>
<td>b7 to b1</td>
<td>7-bit address</td>
</tr>
<tr>
<td>static byte_dt iic_str2</td>
<td>-</td>
<td>Structure to store status</td>
</tr>
<tr>
<td>Structure member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>iic_status</td>
<td>1 byte</td>
<td>All statuses</td>
</tr>
<tr>
<td>iic_start</td>
<td>b0</td>
<td>Mid-communication flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Communication completed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Mid-communication</td>
</tr>
<tr>
<td>iic_err_par</td>
<td>b1</td>
<td>Parameter error flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: No error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Parameter error</td>
</tr>
<tr>
<td>iic_err_nack</td>
<td>b2</td>
<td>NACK detection error flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: No error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: NACK detection error</td>
</tr>
<tr>
<td>iic_err_addr</td>
<td>b3</td>
<td>No address match error flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: No error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: No address match error</td>
</tr>
<tr>
<td></td>
<td>b7 to b4</td>
<td>Not used (undefined)</td>
</tr>
<tr>
<td>unsigned char iic_length</td>
<td>1 byte</td>
<td>Transfer data length</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
<td>1 byte</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>unsigned char far *iic_pointer</td>
<td>4 bytes</td>
<td>Transmit/receive buffer pointer</td>
</tr>
</tbody>
</table>
### 4.2 Function Tables

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void main (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong></td>
<td>Main processing</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>Contents</td>
</tr>
<tr>
<td>unsigned char iic_tx[BUFSIZE]</td>
<td>Transmit buffer</td>
</tr>
<tr>
<td>unsigned char iic_rx[BUFSIZE]</td>
<td>Receive buffer</td>
</tr>
<tr>
<td>unsigned char retry_counter</td>
<td>Count number of communication retries</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Function</strong></td>
<td>After initializing the system clock and UART2, master transmission and reception are repeated alternately. After calling the iic_master_start function to start master control, call the iic_master_end function and wait for master control to be completed. When the iic_master_end function returns ADD_ERR (communication stop because of address not matched error), communication is retried.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void mcu_init (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong></td>
<td>System clock setting</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>Contents</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Function</strong></td>
<td>Call this function from the main processing. Set the system clock (XIN clock).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void uart2_init (unsigned char ini)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong></td>
<td>UART2 initial setting</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>unsigned char ini</td>
<td>0: I2C mode disabled</td>
</tr>
<tr>
<td></td>
<td>1: I2C mode enabled</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>Contents</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td><strong>Function</strong></td>
<td>Call this function from the main processing. Initialize the SFRs used for UART2 in special mode 1 (I2C mode).</td>
</tr>
</tbody>
</table>
### I2C-bus Interface Using UARTi Special Mode 1
(Master Transmit/Receive)

#### Declaration

```c
unsigned char iic_master_start (
    unsigned char addr,
    unsigned char rw,
    unsigned char far *buf,
    unsigned char len)
```

#### Outline

Master control start processing

#### Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char addr</td>
<td>0x00 to 0x7F: Specify slave address</td>
</tr>
<tr>
<td>unsigned char rw</td>
<td>0x00: Master transmit 0x01: Master receive</td>
</tr>
<tr>
<td>unsigned char far *buf</td>
<td>Transmit or receive buffer pointer</td>
</tr>
<tr>
<td>unsigned char len</td>
<td>0x01 to 0xFF: Transfer data length</td>
</tr>
</tbody>
</table>

#### Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>(structure member) iic_status</td>
<td>All statuses</td>
</tr>
<tr>
<td>(structure member) iic_start</td>
<td>Mid-communication flag</td>
</tr>
<tr>
<td>(structure member) iic_err_par</td>
<td>Parameter error flag</td>
</tr>
<tr>
<td>(structure member) iic_slave_addr</td>
<td>Slave address</td>
</tr>
<tr>
<td>unsigned char iic_length</td>
<td>Transfer data length</td>
</tr>
<tr>
<td>unsigned char far *iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
</tbody>
</table>

#### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>BUSY</td>
<td>Bus busy</td>
</tr>
<tr>
<td></td>
<td>RDY</td>
<td>Bus free</td>
</tr>
<tr>
<td></td>
<td>PAR_ERR</td>
<td>Parameter error</td>
</tr>
</tbody>
</table>

#### Function

This function is called by the main function to perform master control start processing. Before executing this function, execute the uart2_init function to enable I2C mode. In the function header, all statuses are initialized and argument parameters are checked. If any parameter value is invalid, the parameter error flag is set to 1 and PAR_ERR is returned. Master control start processing is not performed when a parameter error is detected. Next, the bus status is checked.

- When the bus is busy, the returned value is BUSY and master control start processing is not performed.
- When the bus is free, the returned value is RDY and master control start processing is performed. Set the mid-communication flag to 1 and a start condition is generated.

### Declaration

```c
void _start_stop_condition_detection (void)
```

#### Outline

Start/stop condition generation interrupt handling

#### Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Function

An interrupt is generated when the start condition generation is completed and a stop condition is detected. The sta_int function is called when the start condition generation is completed. The stp_int function is called when a stop condition is detected.
Declaration  static void sta_int (void)

Outline  Start condition detection processing

Argument  
<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

Variable (global)  
<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>(structure member) iic_slave_addr</td>
<td>Slave address</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
</tbody>
</table>

Returned value  
<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Function  Called from the start/stop condition generation interrupt handling. UART2 transmit/receive interrupt is enabled. Transmit the slave address.

Declaration  static void stp_int (void)

Outline  Stop condition detection processing

Argument  
<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

Variable (global)  
<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>(structure member) iic_start</td>
<td>Mid-communication flag</td>
</tr>
</tbody>
</table>

Returned value  
<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Function  Called from the start/stop condition generation interrupt handling. SFR associated with UART2 values which changed during communication are returned to their values, and the mid-communication flag is set to 0.

Declaration  void _uart2_transmit (void)

Outline  UART2 transmit interrupt handling

Argument  
<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

Variable (global)  
<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>(structure member) iic_err_addr</td>
<td>No address match error flag</td>
</tr>
<tr>
<td>(structure member) iic_rw</td>
<td>R/W flag</td>
</tr>
</tbody>
</table>

Returned value  
<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Function  An interrupt is generated at the falling edge of the ninth bit of the SCL clock. Read the U2RB register in the function header. When a NACK is detected during slave address transmission, set the no address match error flag to 1. At all other times, the master_trn_int function is called during master transmission and the master_rcv_int function is called during master reception. When communication is completed, generate a stop condition.
I2C-bus Interface Using UARTi Special Mode 1
(Master Transmit/Receive)

Declaration static unsigned char master_trn_int (unsigned short rb_data)

Outline Master transmit processing

Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned short rb_data</td>
<td>Data read from the U2RB register</td>
</tr>
</tbody>
</table>

Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>(structure member) iic_err_nack</td>
<td>NACK detection error flag</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>unsigned char iic_length</td>
<td>Transfer data length</td>
</tr>
<tr>
<td>unsigned char far *iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
</tbody>
</table>

Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>IIC_SP_ON</td>
<td>0: Stop condition generated</td>
</tr>
<tr>
<td></td>
<td>IIC_SP_OFF</td>
<td>1: Stop condition not generated</td>
</tr>
</tbody>
</table>

Function

Called from the UART2 transmit interrupt handling.
IIC_SP_OFF is returned in the following case:
• ACK is detected and not the last byte (starts the next transmission).
IIC_SP_ON is returned in the following cases:
• NACK is detected (NACK detect error flag is set to 1).
• When the last byte transmission is completed.

Declaration static unsigned char master_rcv_int (unsigned short rb_data)

Outline Master receive processing

Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned short rb_data</td>
<td>Data read from the U2RB register</td>
</tr>
</tbody>
</table>

Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>unsigned char iic_length</td>
<td>Transfer data length</td>
</tr>
<tr>
<td>unsigned char far *iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
</tbody>
</table>

Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>IIC_SP_ON</td>
<td>0: Stop condition generated</td>
</tr>
<tr>
<td></td>
<td>IIC_SP_OFF</td>
<td>1: Stop condition not generated</td>
</tr>
</tbody>
</table>

Function

Called from the UART2 transmit interrupt handling.
The argument value is stored in the receive buffer (except for the slave address data).
NACK is set to the transmit register when the following data is the last byte. ACK is
set to the transmit register when the following data is not the last byte. After setting
ACK or NACK to the transmit register, the next receive operation starts.
IIC_SP_OFF is returned in the following case:
• The following data is not the last byte data.
IIC_SP_ON is returned in the following case:
• The last byte receive operation is completed.
### I2C-bus Interface Using UART Special Mode 1 (Master Transmit/Receive)

**Declaration**

```c
unsigned char iic_master_end (void)
```

**Outline**

Master control completed processing

**Argument**

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

**Variable (global)**

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>(structure member) iic_status</td>
<td>All statuses</td>
</tr>
<tr>
<td>(structure member) iic_start</td>
<td>Mid-communication flag</td>
</tr>
<tr>
<td>(structure member) iic_err_par</td>
<td>Parameter error flag</td>
</tr>
<tr>
<td>(structure member) iic_err_nack</td>
<td>NACK detection error flag</td>
</tr>
<tr>
<td>(structure member) iic_err_addr</td>
<td>No address match error flag</td>
</tr>
</tbody>
</table>

**Returned value**

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>BUSY</td>
<td>Mid-communication</td>
</tr>
<tr>
<td></td>
<td>RDY</td>
<td>Communication completed</td>
</tr>
<tr>
<td></td>
<td>ADDR_ERR</td>
<td>Address not matched</td>
</tr>
</tbody>
</table>

**Function**

Called from the main function. Informs the user of the master control state completed. During communication, this function returns BUSY. When communication is completed, this function returns RDY. Additional processing after communication is completed can be added as needed.
### 4.3 Main Processing

```
main()
asm("fclr I")
```

Disable interrupts.

```
mcsi init()  
```

System clock initial setting (XIN clock setting)

```
uart2_init()  
asm("fset I")
```

UART2 special mode 1 (I²C mode) enabled

Enable interrupts.

```
mode ← WRITE
ret ← BUSY
retry_counter ← 0
```

R/W mode initial setting (master transmit)

Initialize RAM for returned value of iic_master_end.

Initialize retry counter.

```
mode = WRITE?
```

≠ WRITE (master receive)

= WRITE (master transmit)

```
= 0 (bus busy)
= 0 (bus free or parameter error)
```

Master control start processing

```
iic_master_start()
```

Master control completed processing

```
iic_master_end()
```

Switch(ret)

```
= default  
(BUSY: Mid-communication)
= RDY  
(communication completed)
```

Initialize retry counter.

```
retry_counter++
```

Increment retry counter

```
= ADDR_ERR  
(address not matched error)
```

See Note 1

```
mode = WRITE?
```

No

```
mode ← READ
```

Change R/W mode

Yes

```
mode ← WRITE
```

```
ret = BUSY?
```

Yes

Note:

1. Additional processing can be added as needed.
4.4 System Clock Setting

mcu_init()

- PRCR ← 0x03  
  Disable protection.

- PM0 ← 0x00  
  Single-chip mode

- PM1 ← 0x08  
  Internal area expansion: Entire area is usable

- CM2 ← 0x00  
  Start main clock oscillating.

- CM1 ← 0xA0  
  Main clock division: divided-by-4

- CM0 ← 0x08  
  Enable bits CM16 and CM17.

- CM1 ← 0x60  
  Main clock division: divided-by-2

- CM1 ← 0x20  
  Main clock division: no division

- UCLKSELO (1) ← 0x00  
  UART0 to UART2 clock prior to division: f1

- PCLKR ← 0x03  
  UART5 to UART7 clock prior to division: f1

- PRCR ← 0x00  
  SI/O clock: f1SIO

  return

  Enable protection.

Note:
1. The UCLKSELO register may not be existed depending on MCU products.
4.5 UART2 Initial Setting

```c
uart2_init()

ini = 1?

return

ini = 1? (I2C mode enabled)

U2SMR ← 0x01

Select I2C mode.

BCNIC ← 0x00

S2TIC ← 0x00

U2C1 ← 0x00

Disable UART2 transmit interrupt.

U2MR ← 0x02

Select I2C mode, select internal clock.

U2SMR2 ← 0x03

U2SMR3 ← 0x00

S2TIC ← 0x00

S2TIC ← 0x00

U2MR ← 0x00

PD_IIC ← 0x00

BCNIC ← 0x00

PD_IIC & PD_IIC_INIT

Set the initial value: P7_0 (SDA2) = 1 (high)

S2TIC ← 0x00

U2C1 ← 0x00

U2C1 ← 0x10

Select UART2 transmit interrupt, enable clock synchronization.

U2BRG ← IIC_BRG

U2C0 ← 0x90 (1)

SDA2 digital delay: Seven or eight cycles of U2BRG count source

U2BRG count source: f1

Transfer format: MSB first

U2C0 ← 0x90 (1)

Set 384 kbps transfer rate.

Select transmission completed (TXEPT is 1) as UART2 transmit interrupt source.

Note:
1. Ports P7_0 and P7_1 in the M16C/50 Series are not N-channel open drain outputs.
   When using M16C/50 Series, set the NCH bit in the U2C0 register to 1 (pins TDXi/SDAi and SCLi are open drain output) before setting the initial value of SDAi output (P7_0).
```

Note:
1. Ports P7_0 and P7_1 in the M16C/50 Series are not N-channel open drain outputs.
   When using M16C/50 Series, set the NCH bit in the U2C0 register to 1 (pins TDXi/SDAi and SCLi are open drain output) before setting the initial value of SDAi output (P7_0).

Set the port direction: PD7_0 (SDA2) = PD7_1 (SCL2) = 0 (input mode)

Disable start/stop condition generation interrupt.

Disable UART2 transmit interrupt.

Disable transmission/reception.

Disable serial interface.

See Note 1.
### 4.6 Master Control Start Processing

#### Argument

- `addr`: specify slave address
- `rw`: master transmit, master receive
- `buf`: transmit or receive buffer pointer
- `len`: transfer data length

#### Process Flow

1. **iic_master_start()**
   - Clear all statuses.

2. **Parameter error**
   - Check if address or length is incorrect.
   - If so, set parameter error flag to 1 and return.

3. **BBS = 1?**
   - Check if bus is busy.
   - If busy, return bus busy.
   - If free, continue.

4. **Set slave address**
   - Shift address by 1.

5. **Set transfer data length**
   - Update with length.

6. **Set buffer address**
   - Update with buffer pointer.

7. **Set mid-communication flag to 1**

8. **Enable start/stop condition generation interrupt**

9. **Select I2C mode, select internal clock**

10. **Set U2BRG to 0 to set the shortest wait time**

11. **Generate start condition**

**Note:**
1. This process is considered in technical update (TN-16C-130A/EA).
4.7 Start/Stop Condition Generation Interrupt Handling

}\_start\_stop\_condition\_detection()\

\begin{align*}
BBS &= 1? \\
&= 1 \text{ (stop condition detection)} \\
&= 1 \text{ (start condition detection)}
\end{align*}

Start condition detection processing
\begin{itemize}
  \item sta\_int()
\end{itemize}

Stop condition detection processing
\begin{itemize}
  \item stp\_int()
\end{itemize}

return

4.8 Start Condition Detection Processing

sta\_int()

U2SMR3 ← 0xE2
Clock phase: With clock delay
Enable transmission/reception.

U2C1 ← 0x15
Do not generate start/stop conditions.

U2SMR4 ← 0x00
Clear ABT bit.

U2RB ← 0x0000
Set slave address.

\text{temp.byte.byte0 ← iic\_slave\_addr}
Set data to release SDA2 pin at the ninth bit.

\text{temp.byte.byte1 ← 0x01}
Start first byte (slave address) transmission.

U2TB ← temp.all
Set IR bit to 0 after changing CKPH bit.

BCNIC ← 0x01
Enable UART2 transmit interrupt.

iic\_index ← 0x00
Initialize number of transmit/receive bytes.

return
4.9 Stop Condition Detection Processing

stp_int()

U2C1 ← 0x10

P_IIC ← P_IIC | P_IIC_INIT

U2MR ← 0x00

U2SMR3 ← 0xE0

U2SMR4 ← 0x70

U2MR ← 0x02

S2TIC ← 0x00

BCNIC ← 0x00

iic_index ← 0x00

iic_start ← 0

return

- Disable transmission/reception.
- Set the initial value: P7_0 (SDA2) = 1 (high)
- Disable serial interface.
- Set clock phase: No clock delay
- Enable NACK output (release SDA2 pin), enable SCL output stop.
- Select I2C mode, select internal clock.
- Disable UART2 transmit interrupt.
- Disable start/stop condition generation interrupt.
- Initialize number of transmit/receive bytes.
- Set mid-communication flag to 0.
4.10 UART2 Transmit Interrupt Handling

```c
_uart2_transmit()

temp.all ← U2RB

iic_index = 0x00
&& temp.bit.b8 = 1?

ACK detection in slave address or from the second byte on

iic_index = 0x00
&& temp.bit.b8 = 1?

NACK detection in slave address

iic_rw = 0?

= 0 (master transmit)
≠ 0 (master receive)

= 0 (master transmit)
≠ 0 (master receive)

Master receive processing
master_rcv_int()
stop_req ← Returned value

Master transmit processing
master_trn_int()
stop_req ← Returned value

stop_req = IIC_SP_ON?

≠ IIC_SP_ON (stop condition not generated)

= IIC_SP_ON (stop condition generated)

U2SMR4 ← 0x04

U2SMR4 ← 0x3C

return

stop_req ← IIC_SP_ON

stop_req ← Returned value

iic_err_addr ← 1

Set address not matched error flag to 1.

stop_req ← IIC_SP_ON

Generate stop condition.
```

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### 4.11 Master Transmit Processing

```
master_trn_int()

[Argument]
unsigned short rb_data: Data read from the U2RB register

temp.all ← rb_data

Set data read from the receive buffer register.

temp.bit.b8 = 0?

≠ 0 (NACK detection)

= 0 (ACK detection)

iic_index < iic_length?

≥ iic_length (last byte)

< iic_length (not last byte)

iic_index++

Number of transmit/receive bytes + 1

iic_pointer++

Pointer to the transmit buffer + 1

temp.byte.byte0 ← *iic_pointer

temp.byte.byte1 ← 0x01

U2TB ← temp.all

Set transmit data to the U2TB register (start transmission).

return(IIC_SP_OFF)

return(IIC_SP_ON)

Set data read from the U2RB register.

Set data to release the SDA2 pin at the ninth bit.

Set NACK detection error flag to 1.

Set transmit data to the U2TB register.

temp.all

iic_err_nack ← 1

Flag to 1.
### 4.12 Master Receive Processing

![Diagram showing the Master Receive Processing flowchart.]

**Arguments**
- `unsigned short rb_data`: Data read from the U2RB register.

**Flowchart Notes**
- **iic_index = 0x00?**
- **≠ 0x00 (from the second byte on)**
- **iic_index = 0x00?**
- **≠ 0x00 (from the second byte on)**
- **iic_pointer ← (unsigned char)rb_data**
- Store data read from the receive buffer register to the receive buffer.
- Pointer to the receive buffer + 1
- **iic_index ≥ iic_length?**
- **≥ iic_length (last byte)**
- **＜ iic_length (not last byte)**
- **iic_index++ Number of transmit/receive bytes + 1**
- **iic_index ≥ iic_length?**
- **≥ iic_length (last byte)**
- **＜ iic_length (next received data is not the last byte)**
- **U2TB ← 0x01FF**
- **Set NACK for next byte**
- **(prepare for next receive).**
- **return(IIC_SP_OFF)**
- **U2TB ← 0x00FF**
- **Set ACK for next byte**
- **(prepare for next receive).**
- **return(IIC_SP_ON)**

### 4.13 Master Control Completed Processing

![Diagram showing the Master Control Completed Processing flowchart.]

**Flowchart Notes**
- **iic_start = 1?**
- **= 1 (mid-communication)**
- **≠ 1 (communication completed)**
- **(iic_status & 0x0E) = 0x00?**
- **= 0x00 (normal end)**
- **≠ 0x00 (error)**
- **iic_addr_err = 1?**
- **Yes**
- **return(ADDR_ERR)**
- **No**
- **See Note 1.**
- **See Note 2.**
- **return(RDY)**
- **return(BUSY)**

**Notes:**
1. Additional processing of communication completed normally can be added as needed.
2. Additional processing of communication completed with error can be added as needed.
5. Sample Program

A sample program can be downloaded from the Renesas Electronics website. To download, click “Application Notes” in the left-hand side menu of the M16C Family page.

6. Reference Documents

Application Note

M16C Family I2C-Bus Interface Using UARTi Special Mode 1
(REJ05B1349-0100)
The latest version can be downloaded from the Renesas Electronics website.

M16C/63 Group User’s Manual: Hardware Rev.1.00
M16C/64 Group User’s Manual: Hardware Rev.1.05
M16C/64A Group User’s Manual: Hardware Rev.1.10
M16C/64C Group User’s Manual: Hardware Rev.0.10
M16C/65 Group User’s Manual: Hardware Rev.1.10
M16C/65C Group User’s Manual: Hardware Rev.0.10
M16C/6C Group User’s Manual: Hardware Rev.1.00
M16C/5LD Group, M16C/56D Group User’s Manual: Hardware Rev.1.10
M16C/5L Group, M16C/56 Group User’s Manual: Hardware Rev.1.00
M16C/5M Group, M16C/57 Group User’s Manual: Hardware Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

Technical News/Technical Update
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
## Revision History

<table>
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<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>1.00</td>
<td>Aug 31, 2010</td>
<td>First edition issued</td>
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<tr>
<td>1.01</td>
<td>Jan 31, 2011</td>
<td>Add M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/56D, M16C/56, M16C/57</td>
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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
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