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April 1st, 2010  
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M16C/65 Group

Long-period timers

1. Abstract

In this process, Timer A0 and Timer A1 are connected to make a 16-bit timer with a 16-bit prescaler. Use the following peripheral function:

- Timer mode of timer A
- Event counter mode of timer A

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Introduction

(1) Set timer A0 to timer mode, and set timer A1 to event counter mode.

(2) Perform a count on count source TIMAB using timer A0 to count for 1 ms, and perform a count on timer A0 using timer A1 to count for 1 second.

(3) Connect a 20MHz oscillator to XIN.

(4) Using POFSi bit in TAPOFS register to select the output polarity of the TAiOUT pin.

4. Operation

(1) Setting the count start flag to “1” causes the counter to begin counting. The counter of timer A0 performs a down count on count source TIMAB.

(2) If the counter of timer A0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A0 interrupt request bit goes to “1”. The counter of timer A1 performs a down count on underflows in timer A0.

(3) If the counter of timer A1 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A1 interrupt request bit goes to “1”.
Figure 1 shows the operation timing.

Figure 2 shows the connection diagram.
5. Set-up procedure

Table 1 shows Timer A count source, Figure 3 shows block diagram of Timer A count source in timer mode.

### Table 1. Count Source Selection of Timer A

<table>
<thead>
<tr>
<th>TCKDIVC0 register (Note 1)</th>
<th>TACSj register (Note 2)</th>
<th>TAiMR register</th>
<th>Count source</th>
<th>Count source period</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCDIV00</td>
<td>TCS3/ TCS7</td>
<td>TCS2/ TCS6</td>
<td>TCS1/ TCS5</td>
<td>TCS0/ TCS4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-</td>
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</table>

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

Note 3: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.
Figure 3. Count source of Timer A

Setting timer A0

Selecting a clock used prior to timer AB frequency dividing
(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.)

Clock select prior to timer AB division bit
0 : f1

Reserved bits
Set to 0

No register bits. If necessary, set to 0. Read as undefined value.

Reserved bits
Set to 0
## Selecting timer mode and functions

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
<th>TA0 count source select bit (Note1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled</td>
</tr>
</tbody>
</table>

**Timer A0 mode register** [Address 0036h]  
**TA0MR**

- **Selection of timer mode**
- **Pulse output function select bit**
- **Gate function select bit**

- **Count source select bit (Note1)**
  - 0 : TCS3 bit or TCS7 bit in register TA0C0 to TA0C2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 1.
  - Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

## Setting counter value

<table>
<thead>
<tr>
<th>(b15)</th>
<th>b7</th>
<th>4Eh</th>
<th>(b8)</th>
<th>b7</th>
<th>1Fh</th>
<th>b0</th>
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**Timer register** [Address 0327h, 0326h]  
**TA0**
Selecting event counter mode and functions

- **Timer A1 mode register [Address 0337h]**
  - **TA1MR**
  
  - Selection of event counter mode
  
  - **Pulse output function select bit**
    - 0: Pulse is not output (TA1OUT pin is a normal port pin)
  
  - **Counter polarity select bit**
    - 0: Counts external signal's falling edge
  
  - **Up/down switching cause select bit**
    - 0: Up/down signal's content
  
  - 0 (Must always be "0" in event counter mode)
  
  - **Count operation type select bit**
    - 0: Reload type

Setting trigger select register

- **Trigger select register [Address 0323h]**
  - **TRGSR**
  
  - **Timer A1 event/trigger select bit**
    - b1 b0
    - 1 0: TA0 overflow or underflow is selected

Setting counter value

- **Timer register [Address 0329h, 0328h]**
  - **TA1**
  
  - **03h E7h**
  
  - **TA1OUT output polar control bit**
    - 0: Output waveform "H" active

Selecting waveform output function

- **Timer A waveform output function select register [Address 01D5h]**
  - **TAPOFS**
  
  - **TA1OUT output polar control bit**
    - 0: Output waveform "H" active

Setting count start flag

- **Count start flag [Address 0320h]**
  - **TABSr**
  
  - **Timer A0 count start flag**
    - **Timer A1 count start flag**

**Start count**
6. Reference

Hardware manual
M16C/65 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
(Use the most recent version of the document on the Renesas Technology Web site.)

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## Revision

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<td>2009.10</td>
<td>-</td>
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