1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 3.1. Operations of the marked items are described below. The examples are explained below using the M16C/65 Group.

2. Introduction

This application note is applied to the following MCUs:

MCU(s): M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Chosen functions

Table 3.1 Chosen Functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock prior to division select</td>
<td>✓ f1</td>
<td>Transfer format</td>
<td>✓ LSB first</td>
</tr>
<tr>
<td></td>
<td>fOCO-F</td>
<td></td>
<td>MSB first</td>
</tr>
<tr>
<td>Peripheral clock</td>
<td>✓ f1SIO</td>
<td>Transmission interrupt factor</td>
<td>✓ Transmission buffer empty</td>
</tr>
<tr>
<td></td>
<td>f2SIO</td>
<td></td>
<td>Transmission complete</td>
</tr>
<tr>
<td>Transfer clock source</td>
<td>✓ Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)</td>
<td>Output transfer clock to multiple pins (1)</td>
<td>✓ Not selected</td>
</tr>
<tr>
<td></td>
<td>External clock (CLKi pin)</td>
<td></td>
<td>Selected</td>
</tr>
<tr>
<td>CTS function</td>
<td>✓ CTS function enabled</td>
<td>Serial data logic</td>
<td>✓ No reverse</td>
</tr>
<tr>
<td></td>
<td>CTS function disable</td>
<td></td>
<td>Reverse</td>
</tr>
<tr>
<td>CLK polarity</td>
<td>✓ Output transmission data at the falling edge of the transfer clock</td>
<td>Separate CTS/RTS pins (2)</td>
<td>✓ Shared pin</td>
</tr>
<tr>
<td></td>
<td>Output transmission data at the rising edge of the transfer clock</td>
<td>Separated CTS/RTS pins (2)</td>
<td>Separated</td>
</tr>
</tbody>
</table>

Notes:
1. This can be selected only when UART1 is used in combination with the internal clock.
2. This function separates CTS0/RTS0, outputs RTS0 from the P6_0 pin, and inputs CTS0 from the P6_4 pin. When this function is selected, UART1 CTS/RTS function can not be utilized. Set the UART1 CTS/RTS disable bit to “1”.

4. Operation

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.
(2) When input to the CTSi pin goes to “L” level, transmission starts (the CTSi pin must be controlled on the reception side).
(3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to “1”. Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
(4) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that transmission is completed. The transfer clock goes at “H” level.
(5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.
Figure 4.1 shows the operation timing.

Example of wiring

![Diagram of wiring](Note)

Example of operation

![Timing diagram](Note)

<table>
<thead>
<tr>
<th>Event</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>Transmission enabled</td>
</tr>
<tr>
<td>(2)</td>
<td>Confirming CTS</td>
</tr>
<tr>
<td>(3)</td>
<td>Start transmission</td>
</tr>
<tr>
<td>(4)</td>
<td>Transmission is complete</td>
</tr>
<tr>
<td>(5)</td>
<td>Transmit next data</td>
</tr>
</tbody>
</table>

The above timing applies to the following settings:
- Internal clock is selected.
- CTS function is selected.
- CLK polarity select bit = “0”.
- Transmit interrupt cause select bit = “0”.

Note: Since TxD2 pin is N-channel open drain, this pin needs pull-up resistor.
5. Set-up Procedure

Setting UART clock select register
(Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)

- UART clock select register [Address 0252h] UCLKSEL0
- UART0 to UART2 clock prior to division select bit
  - 0 : f1
- UART5 to UART7 clock prior to division select bit
  - 0 : f1

Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)

- UART0 transmit/receive mode register [Address 0248h] U0MR
- UART1 transmit/receive mode register [Address 0258h] U1MR
- UART2 transmit/receive mode register [Address 0268h] U2MR
- UART5 transmit/receive mode register [Address 0288h] U5MR
- UART6 transmit/receive mode register [Address 0298h] U6MR
- UART7 transmit/receive mode register [Address 02A8h] U7MR

- Must be fixed to “001”
- Internal/external clock select bit
  - 0 : Internal clock
- Invalid in clock synchronous I/O mode
- Invalid in clock synchronous I/O mode
- Invalid in clock synchronous I/O mode
- TxD, RxD I/O polarity reverse bit
  - Usually set to “0”
### Setting UART transmit/receive control register (i = 0 to 2, 5 to 7)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **UART0 transmit/receive control register** [Address 024Ch] U0C0
- **UART1 transmit/receive control register** [Address 025Ch] U1C0
- **UART2 transmit/receive control register** [Address 026Ch] U2C0
- **UART5 transmit/receive control register** [Address 028Ch] U5C0
- **UART6 transmit/receive control register** [Address 029Ch] U6C0
- **UART7 transmit/receive control register** [Address 02ACh] U7C0

#### CTS/RTS function select bit (Valid when bit4 = "0")

- 0 : CTS function is selected (Note2)
- 0 : f1SIO is selected
- 1 : f2SIO is selected
- 1 : Do not set to this value

#### UBRG count source select bit

- 0 0 : f1SIO or f2SIO is selected (Note1)
- 0 1 : f8SIO is selected
- 1 0 : f32SIO is selected
- 1 1 : Do not set to this value

#### CTS/RTS disable bit

- 0 : CTS/RTS function enabled

#### Transmit register empty flag

- 0 : Data present in transmit register (during transmission)
- 1 : No data present in transmit register (transmission completed)

#### Data output select bit

- 0 : Pins TxDi/SDAi and SCLi are CMOS output
- 1 : Pins TxDi/SDAi and SCLi are N-channel open-drain output

#### CLK polarity select bit

- 0 : Transmission data is output at falling edge of transfer clock and reception data is input at rising edge

#### Transfer format select bit

- 0 : LSB first

---

**Note 1:** When the PCLK1 bit in the PCLKR register is "1", the selected clock source is f1SIO. When the PCLK1 bit is "0", the selected clock source is f2SIO.

**Note 2:** Set the corresponding port direction register to "0" (input mode).

---

### Setting UART transmit/receive control register 2

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **UART transmit/receive control register 2** [Address 0250h] UCON

#### UART0 transmit interrupt cause select bit

- 0 : Transmit buffer empty (TI = 1)

#### UART1 transmit interrupt cause select bit

- 0 : Transmit buffer empty (TI = 1)

#### Valid when bit5 = "1"

#### UART1 CLK/CLKS select bit 1

- 0 : CLK output is only from CLK1

#### Separate UART0 CTS/RTS bit

- 0 : CTS/RTS shared pin
Setting UART\textsubscript{i} transmit/receive control register 1 (i = 0 to 2, 5 to 7)

UART\textsubscript{0} transmit/receive control register 1 [Address 024Dh] U0C1
UART\textsubscript{1} transmit/receive control register 1 [Address 025Dh] U1C1

- **Data logic select bit**
  - 0 : No reverse
- **Error signal output enable bit**
  - Must always be “0” in clock synchronous I/O mode

UART\textsubscript{2} transmit/receive control register 1 [Address 026Dh] U2C1
UART\textsubscript{5} transmit/receive control register 1 [Address 028Dh] U5C1
UART\textsubscript{6} transmit/receive control register 1 [Address 029Dh] U6C1
UART\textsubscript{7} transmit/receive control register 1 [Address 02ADh] U7C1

- **UART\textsubscript{i} transmit interrupt source select bit**
  - 0 : Transmit buffer register empty (TI = 1)
- **Data logic select bit**
  - 0 : No reverse
- **Error signal output enable bit**
  - Must always be “0” in clock synchronous I/O mode

Setting UART\textsubscript{i} bit rate register (i = 0 to 2, 5 to 7)

UART\textsubscript{0} bit rate register [Address 0249h] U0BRG
UART\textsubscript{1} bit rate register [Address 0259h] U1BRG
UART\textsubscript{2} bit rate register [Address 0269h] U2BRG
UART\textsubscript{5} bit rate register [Address 0289h] U5BRG
UART\textsubscript{6} bit rate register [Address 0299h] U6BRG
UART\textsubscript{7} bit rate register [Address 02A9h] U7BRG

- **Data logic select bit**
  - 0 : No reverse
- **Error signal output enable bit**
  - Must always be “0” in clock synchronous I/O mode

Can be set to 00h to FFh (Note)

Setting UART\textsubscript{i} transmit/receive control register 1 (i = 0 to 2, 5 to 7)

Transmission enabled

UART\textsubscript{0} transmit/receive control register 1 [Address 024Dh] U0C1
UART\textsubscript{1} transmit/receive control register 1 [Address 025Dh] U1C1

- **Transmit enable bit**
  - 1 : Transmission enabled

UART\textsubscript{2} transmit/receive control register 1 [Address 026Dh] U2C1
UART\textsubscript{5} transmit/receive control register 1 [Address 028Dh] U5C1
UART\textsubscript{6} transmit/receive control register 1 [Address 029Dh] U6C1
UART\textsubscript{7} transmit/receive control register 1 [Address 02ADh] U7C1

- **Transmit enable bit**
  - 1 : Transmission enabled

Note: Write to the UiBRG register while serial interface is neither transmitting nor receiving. Use MOV instruction to write to the UiBRG register. Write to the UiBRG register after setting bits CLK1 to CLK0 in the UIC0 register.
Writing transmit data

UAR0 transmit buffer register [Address 024Bh, 024Ah] U0TB
UAR1 transmit buffer register [Address 025Bh, 025Ah] U1TB
UAR2 transmit buffer register [Address 026Bh, 026Ah] U2TB
UAR5 transmit buffer register [Address 028Bh, 028Ah] U5TB
UAR6 transmit buffer register [Address 029Bh, 029Ah] U6TB
UAR7 transmit buffer register [Address 02ABh, 02AAh] U7TB

Setting transmission data

When CTSi input level = “L”

Start transmission

Checking the status of UARTi transmit/receive control register (i = 0 to 2, 5 to 7)

UART0 transmit/receive control register [Address 024Dh] U0C1
UART1 transmit/receive control register [Address 025Dh] U1C1
UART2 transmit/receive control register [Address 026Dh] U2C1
UART5 transmit/receive control register [Address 028Dh] U5C1
UART6 transmit/receive control register [Address 029Dh] U6C1
UART7 transmit/receive control register [Address 02ADh] U7C1

Transmit buffer empty bit
0 : Data present in transmit buffer register
1 : No data present in transmit buffer register (Writing next transmit data enable)

Writing next transmit data

UAR0 transmit buffer register [Address 024Bh, 024Ah] U0TB
UAR1 transmit buffer register [Address 025Bh, 025Ah] U1TB
UAR2 transmit buffer register [Address 026Bh, 026Ah] U2TB
UAR5 transmit buffer register [Address 028Bh, 028Ah] U5TB
UAR6 transmit buffer register [Address 029Bh, 029Ah] U6TB
UAR7 transmit buffer register [Address 02ABh, 02AAh] U7TB

Transmission is complete
6. Sample Code  
Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents  
M16C/63 Group User’s Manual: Hardware Rev.2.00  
M16C/64A Group User’s Manual: Hardware Rev.2.00  
M16C/64C Group User’s Manual: Hardware Rev.1.00  
M16C/65 Group User’s Manual: Hardware Rev.2.00  
M16C/65C Group User’s Manual: Hardware Rev.1.00  
M16C/6C Group User’s Manual: Hardware Rev.2.00  
M16C/5LD Group, M16C/56D Group User’s Manual: Hardware Rev.1.10  
M16C/5L Group, M16C/56 Group User’s Manual: Hardware Rev.1.00  
M16C/5M Group, M16C/57 Group User’s Manual: Hardware Rev.1.01  
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News  
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual  
M16C Series, R8C Family C Compiler Package V.5.45  
C Compiler User’s Manual Rev.2.00  
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support  
Renesas Electronics website  
http://www.renesas.com/  

Inquiries  
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## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Sep. 27, 2009</td>
<td>— First edition issued</td>
</tr>
<tr>
<td>1.01</td>
<td>Apr. 28, 2011</td>
<td>— Add: M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/5M, and M16C/57</td>
</tr>
</tbody>
</table>

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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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