1. **Abstract**

   This document describes an example of slave reception using serial interface special mode 2.

2. **Introduction**

   The application example described in this document applies to the following microcomputers (MCUs):

   - MCUs: M16C/63 Group, M16C/64A Group, M16C/65 Group, M16C/65C Group, M16C/6C Group, M16C/5LD Group, M16C/5L Group, M16C/5M Group

   This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the user’s manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. **Operation Confirmation Conditions**

Table 3.1 lists the Operation Confirmation Conditions.

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>M16C/65 Group</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• Main clock: 8 MHz</td>
</tr>
<tr>
<td></td>
<td>• CPU clock: 32 MHz (PLL clock divided by 2 and multiply-by-8)</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (operation enabled from 2.7 to 5.5 V)</td>
</tr>
<tr>
<td>Integrated development</td>
<td>Renesas Electronics</td>
</tr>
<tr>
<td>environment</td>
<td>High-performance Embedded Workshop Version 4.07</td>
</tr>
<tr>
<td>C compiler</td>
<td>Renesas Electronics</td>
</tr>
<tr>
<td></td>
<td>M16C Series, R8C Family C Compiler Package V.5.45 Release 01</td>
</tr>
<tr>
<td>Compile options</td>
<td>-c -finfo -dir &quot;$(CONFIGDIR)&quot;</td>
</tr>
<tr>
<td></td>
<td>The default settings of the integrated development environment are used.</td>
</tr>
</tbody>
</table>
4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P8_2 / INT0</td>
<td>Input</td>
<td>Port to control data reception</td>
</tr>
<tr>
<td>P7_2 / CLK2</td>
<td>Input</td>
<td>Transmit/receive clock input</td>
</tr>
<tr>
<td>P7_1 / RXD2</td>
<td>Input</td>
<td>Serial data input</td>
</tr>
<tr>
<td>P7_0 / TXD2</td>
<td>Output</td>
<td>Serial data output</td>
</tr>
</tbody>
</table>

4.2 Circuit Diagram

Figure 4.1 shows a Master and Slave Connection Example.

Notes:
1. This is used as an N-channel open drain output for the M16C/60 Series.
2. This is used as a CMOS output for the M16C/50 Series. Set the NCH bit in the U2C0 register.
3. Pull individual pins high when they are connected.
5. Software

5.1 Specifications

The sample code performs slave reception of 1-byte data. When the falling edge is input to the INT0 pin, the transmission and reception of UART2 is enabled. After 1-byte data is received, the received data is stored to relocatable variables in the UART2 received interrupt. When the rising edge is input to the INT0 pin, the transmission and reception of UART2 and the serial interface are disabled. Table 5.1 lists the Sample Code Specifications.

Table 5.1 Sample Code Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Slave (Without Clock Delay)</th>
<th>Slave (With Clock Delay)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication mode</td>
<td>Special mode 2 (external clock)</td>
<td>The CKPH bit in the U2SMR3 register is 0 (no clock delay). The CKPOL bit in the U2C0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge).</td>
</tr>
<tr>
<td>Clock phase</td>
<td>The CKPH bit in the U2SMR3 register is 1 (with clock delay).</td>
<td>The CKPH bit in the U2SMR3 register is 1 (with clock delay).</td>
</tr>
<tr>
<td>Data format</td>
<td>Character length: 8 bits</td>
<td></td>
</tr>
<tr>
<td>Bit order</td>
<td>LSB first</td>
<td></td>
</tr>
<tr>
<td>Transmit/receive control</td>
<td>P8_2 pin (INT0 pin)</td>
<td></td>
</tr>
<tr>
<td>Interrupts</td>
<td>• UART2 reception interrupt (priority level: 2)</td>
<td>• INT0 interrupt (priority level: 1)</td>
</tr>
</tbody>
</table>

5.2 Notes

When the following conditions apply, execute the countermeasure listed in “5.3 Operation”.

• When the CKPOL bit in the UiC0 register is 0, and CKPH bit in the UiSMR3 register is 1 (i = 0 to 2 and 5 to 7).
• When the CKPOL bit is 1, and CKPH bit is 0.

When the CKPOL bit is 0 and the CKPH bit is 1 (with clock delay), the CLKi pin is low while the communication path is idle (when the CKPOL bit is 1 and CKPH bit is 0, the CLKi pin is high).
5.3 Operation With No Clock Delay

Figure 5.1 shows an Example of Slave Transmission/Reception Using Special Mode 2 With No Clock Delay, and Table 5.2 lists the Measurement Values Using the Sample Code.

(1) The INT0 interrupt (SS input) is generated.

(2) When the INT0 pin is low:

(2-1) The U2MR register is set to 09h (clock synchronous serial I/O mode, external clock). (The TXD pin becomes output hereat.)

(2-2) The U2C1 register is set to 05h (transmission and reception enabled).

(2-3) Data is written to the U2TB register. (1)

(3) When the INT0 pin is high:

(3-1) The U2C1 register is set to 00h (transmission and reception disabled).

(3-2) The U2MR register is set to 00h (serial interface disabled). (2) (The TXD pin is released hereat.)

(4) When the received data is transferred to the U2RB register, the RI bit in the U2C1 register becomes 1 and a reception interrupt is generated.

(5) Data is read from the U2RB register in the reception interrupt.

Notes:

1. Until process (2-3) is done, do not input the transmit/receive clock to the CLK2 pin.
2. Until the serial interface is disabled, the TXD2 pin retains the last data.
Table 5.2 Measured Values Using the Sample Code (1)

<table>
<thead>
<tr>
<th>Item</th>
<th>Measured Value</th>
<th>Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_s$</td>
<td>Approximately 4.6 $\mu$s</td>
<td>Approximately 147 cycles</td>
</tr>
<tr>
<td>$t_{thold}$</td>
<td>Approximately 4.4 $\mu$s</td>
<td>Approximately 141 cycles</td>
</tr>
<tr>
<td>Time for data reception complete interrupt handling</td>
<td>Approximately 2.6 $\mu$s</td>
<td>Approximately 83 cycles</td>
</tr>
</tbody>
</table>

Note:
1. The conditions for measuring the values are the same as “3. Operation Confirmation Conditions”.
2. The measured values and number of cycles are modified depending on the compiler option settings and interrupt generation timing.

Figure 5.1 Example of Slave Transmission/Reception Using Special Mode 2 With No Clock Delay
5.4 Operation With Clock Delay

Figure 5.2 shows an Example of Slave Transmission/Reception Using Special Mode 2 With a Clock Delay, and Table 5.3 lists the Measured Values Using the Sample Code.

1. The INT0 interrupt (SS input) is generated.
2. When the INT0 pin is low:
   2-1) The U2MR register is set to 0Dh (UART mode, external clock).
       (1) (The TXD pin becomes output hereat.)
   2-2) The U2Cl register is set to 05h (transmission and reception enabled).
   2-3) Data is written to the U2TB register. (1)
   2-4) The U2MR register is set to 09h (clock synchronous serial I/O mode). (2)
3. When the INT0 pin is high:
   3-1) The U2C1 register is set to 00h (transmission and reception disabled).
   3-2) The U2MR register is set to 00h (serial interface disabled). (3) (The TXD pin is released hereat.)
4. When the received data is transferred to the U2RB register, the RI bit in the U2C1 register becomes 1 and the reception interrupt occurs.
5. Data is read from the U2RB register in the reception interrupt handling.

Notes:
1. UART mode is set due to the countermeasure in “5.3 Operation With No Clock Delay”.
2. Until process (2-4) is done, do not input the transmit/receive clock to the CLK2 pin.
3. Until the serial interface is disabled, the TXD2 pin retains the last data.
Figure 5.2 Example of Slave Transmission/Reception Using Special Mode 2 With a Clock Delay

Table 5.3 Measured Values Using the Sample Code (1)

<table>
<thead>
<tr>
<th>Item</th>
<th>Measured Value</th>
<th>Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>ts</td>
<td>Approximately 4.8 μs</td>
<td>Approximately 153 cycles</td>
</tr>
<tr>
<td>thold</td>
<td>Approximately 4.4 μs</td>
<td>Approximately 141 cycles</td>
</tr>
<tr>
<td>Time for data reception complete interrupt handling</td>
<td>Approximately 2.6 μs</td>
<td>Approximately 83 cycles</td>
</tr>
</tbody>
</table>

Note:
1. The conditions for measuring the values are the same as “3. Operation Confirmation Conditions”.
   The measured values and number of cycles are modified depending on the compiler option settings and interrupt generation timing.
5.5 Constants

Table 5.4 lists the Constants Used in the Sample Code.

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>OVR_ERROR_MASK</td>
<td>1000h</td>
<td>Confirms an overrun error.</td>
</tr>
<tr>
<td>OVR_ERROR</td>
<td>1000h</td>
<td>Overrun error</td>
</tr>
<tr>
<td>HIGH</td>
<td>1</td>
<td>Determines a rising edge.</td>
</tr>
<tr>
<td>LOW</td>
<td>0</td>
<td>Determines a falling edge.</td>
</tr>
<tr>
<td>DUMMY_DATA</td>
<td>55h</td>
<td>Dummy data for transmission.</td>
</tr>
<tr>
<td>SUCCESS</td>
<td>00h</td>
<td>Success</td>
</tr>
<tr>
<td>ERROR</td>
<td>FFh</td>
<td>Error</td>
</tr>
</tbody>
</table>

5.6 Variables

Table 5.5 lists the Variables.

<table>
<thead>
<tr>
<th>Style</th>
<th>Variable Name</th>
<th>Content</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>rcv_data</td>
<td>Stores received data.</td>
<td>uart2_receive()</td>
</tr>
<tr>
<td></td>
<td>u2_overrun</td>
<td>Stores an overrun error result.</td>
<td>main()</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>_uart2_receive()</td>
</tr>
</tbody>
</table>

5.7 Function Tables

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void mcu_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>CPU clock setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>Contents</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>Function</td>
<td>Set the PLL clock as the CPU clock. Set the main clock as the CPU clock when using the M16C/63 Group.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void peripheral_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Peripheral initial setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>Contents</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td>Meaning</td>
</tr>
<tr>
<td>Function</td>
<td>Perform initial setting of UART2. Set the NCH bit in the U2C0 register to 1 (pins TXD2/SDA2 and SCL2 are N-channel open drain output) when using the M16C/50 Series. Configure the INT0 interrupt.</td>
</tr>
</tbody>
</table>
### INT0 Interrupt Handling

**Argument**  
Argument name: None  
Meaning: -

**Variable (global)**  
Variable name: None  
Contents: -

**Returned value**  
Type: None  
Value: -  
Meaning: -

**Function**  
At the beginning of the INT0 interrupt handling, sample the input level three times. When a falling edge is input, start the UART2 transmission/reception. When a rising edge is input, disable the serial interface.

### UART2 Receive Interrupt Handling

**Argument**  
Argument name: None  
Meaning: -

**Variable (global)**  
Variable name: r(cv_data)  
Contents: Store received data.  
Variable name: u2_overrun  
Contents: Store overrun error result.

**Returned value**  
Type: None  
Value: -  
Meaning: -

**Function**  
Check to see if an overrun error has been generated, and store the received data to the variables.
5.8 Flowcharts

5.8.1 Main Function

Figure 5.3 shows the Main Function.

![Flowchart of Main Function]

Note:
1. The sample code does not include any processing for when errors occur. Add processing is necessary.

Figure 5.3 Main Function
### 5.8.2 Peripheral Initial Setting

These settings set UART2 and configure the INT0 interrupt. Figure 5.4 shows the Peripheral Initial Setting.

![Peripheral Initial Setting Diagram](image)

<table>
<thead>
<tr>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Interface</td>
<td>Serial Interface</td>
</tr>
<tr>
<td>UART2 to clock synchronous serial I/O mode.</td>
<td>Set UART2 to clock synchronous serial I/O mode.</td>
</tr>
<tr>
<td>Bits SMD2 to SMD0 = ( 001b )</td>
<td>Clock synchronous serial I/O mode</td>
</tr>
<tr>
<td>CKDIR bit = 1</td>
<td>External clock</td>
</tr>
<tr>
<td>U2SMR register initial setting</td>
<td>U2SMR register ( \leftarrow 00h )</td>
</tr>
<tr>
<td>U2SMR2 register initial setting</td>
<td>U2SMR2 register ( \leftarrow 00h )</td>
</tr>
<tr>
<td>Set no clock delay to the UART2 clock phase.</td>
<td>U2SMR3 register ( \leftarrow 00h )</td>
</tr>
<tr>
<td>No clock delay</td>
<td></td>
</tr>
<tr>
<td>U2SMR4 register initial setting</td>
<td>U2SMR4 register ( \leftarrow 00h )</td>
</tr>
<tr>
<td>UART2 associated register settings</td>
<td>U2C0 register ( \leftarrow 10h )</td>
</tr>
<tr>
<td>Bits CLK1 to CLK0 = ( 00b )</td>
<td>f1SIO</td>
</tr>
<tr>
<td>CRD bit = 1</td>
<td>CTS/RTS function disabled</td>
</tr>
<tr>
<td>NCH bit = ( 0^\text{(1)} )</td>
<td>Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge</td>
</tr>
<tr>
<td>CKPOL bit = ( 0^\text{(1)} )</td>
<td>Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge</td>
</tr>
<tr>
<td>UFORM bit = ( 0^\text{(1)} )</td>
<td>LSB first</td>
</tr>
<tr>
<td>Disable UART2 transmission/reception.</td>
<td>U2C1 register ( \leftarrow 10h )</td>
</tr>
<tr>
<td>TE bit = ( 0^\text{(1)} )</td>
<td>Transmission disabled</td>
</tr>
<tr>
<td>RE bit = ( 0^\text{(1)} )</td>
<td>Reception disabled</td>
</tr>
<tr>
<td>Disable the UART2 transmit interrupt.</td>
<td>U2TIC register ( \leftarrow 00h )</td>
</tr>
<tr>
<td>Bits ILVL2 to ILVL0 = ( 000b )</td>
<td>Level 0 (interrupt disabled)</td>
</tr>
<tr>
<td>Enable the UART2 receive interrupt.</td>
<td>U2RIC register ( \leftarrow 02h )</td>
</tr>
<tr>
<td>Bits ILVL2 to ILVL0 = ( 010b )</td>
<td>Level 2</td>
</tr>
<tr>
<td>Select the INT0 interrupt polarity.</td>
<td>IFSR0 bit ( \leftarrow \text{1}^\text{(1)} )</td>
</tr>
<tr>
<td>Both edges</td>
<td></td>
</tr>
<tr>
<td>Enable the INT0 interrupt.</td>
<td>INT0IC register ( \leftarrow 01h )</td>
</tr>
<tr>
<td>Bits ILVL2 to ILVL0 = ( 001b )</td>
<td>Level 1</td>
</tr>
</tbody>
</table>

**Notes:**
1. Ports P7_0 and P7_1 in the M16C/50 Series are not N-channel open drain outputs. Set the NCH bit in the U2C0 register to 1 (pins TDX2/SDA2 and SCL2 are N-channel open drain output) when the M16C/50 Series is used.
2. Set the CKPH bit to 1 when using a clock delay.

**Figure 5.4 Peripheral Initial Setting**
5.8.3 **INT0 Interrupt Function**

When a falling edge is input, UART2 transmission/reception enabled is set. When a rising edge is input, the serial interface is disabled.

Figure 5.5 shows the INT0 Interrupt Function With No Clock Delay, and Figure 5.6 shows the INT0 Interrupt Function With Clock Delay.

---

**Figure 5.5 INT0 Interrupt Function With No Clock Delay**

At the falling edge?
- Sample the input level three times.

At the rising edge
- Match three input level samples to remove noise.

1. **Set the UART2 transmit/receive mode register to clock synchronous serial I/O mode.**
   - **U2MR register ← 09h**
   - Bits SMD2 to SMD0 = 001b: Clock synchronous serial I/O mode
   - CKDIR bit = 1: External clock

2. **Set UART2 to transmission and reception enabled.**
   - **U2C1 register ← 15h**
   - TE bit = 1: Transmission enabled
   - RE bit = 1: Reception enabled

3. **Write dummy data to the transmit buffer.**

4. **Set UART2 to transmission and reception disabled.**
   - **U2C1 register ← 10h**
   - TE bit = 0: Transmission disabled
   - RE bit = 0: Reception disabled

5. **Set the UART2 transmit/receive mode register to serial interface disabled.**
   - **U2MR register ← 00h**
   - Bits SMD2 to SMD0 = 000b: Serial interface disabled

6. **return**
Figure 5.6  INTO Interrupt Function With Clock Delay

<table>
<thead>
<tr>
<th>Function</th>
<th>Register/Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample the input level three times.</td>
<td>U2TB register</td>
<td>Match three input level samples to remove noise.</td>
</tr>
<tr>
<td>At the falling edge?</td>
<td>U2C1 register</td>
<td>At the falling edge</td>
</tr>
<tr>
<td>Set UART2 to transmission and reception</td>
<td>U2C1 register</td>
<td>Set UART2 to transmission and reception disabled.</td>
</tr>
<tr>
<td>Set the UART2 transmit/receive mode register</td>
<td>U2MR register</td>
<td>Set the UART2 transmit/receive mode register to serial interface disabled.</td>
</tr>
<tr>
<td>Set UART2 transmit/receive mode register</td>
<td>U2MR register</td>
<td>Set UART2 transmit/receive mode register to UART mode character bit length is 8 bits.</td>
</tr>
<tr>
<td>Set UART2 to transmission and reception</td>
<td>U2C1 register</td>
<td>Set UART2 to transmission and reception enabled.</td>
</tr>
<tr>
<td>Write dummy data to the transmit buffer.</td>
<td>U2TB register</td>
<td>Write dummy data to the transmit buffer.</td>
</tr>
<tr>
<td>Set the UART2 transmit/receive mode register</td>
<td>U2MR register</td>
<td>Set the UART2 transmit/receive mode register to clock synchronous serial I/O mode.</td>
</tr>
</tbody>
</table>

Note:
1. Transmission and reception start conditions are not satisfied because the CLK2 pin becomes low when the CKPOL bit in the U2C0 register is 0, and the CKPH bit in the U2SMR3 register is 1. Therefore, the UART mode setting is added here.
5.8.4 UART2 Reception Interrupt Function

This function checks whether an overrun error has occurred or not, and stores the received data to the variable. Figure 5.7 shows the UART2 Reception Interrupt Function.

![Diagram of UART2 Reception Interrupt Function]

Figure 5.7 UART2 Reception Interrupt Function
6. Sample Program
A sample program can be downloaded from the Renesas Electronics website.

7. Reference Documents
M16C/65 User’s Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support
Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Dec. 28, 2010</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

All trademarks and registered trademarks are the property of their respective owners.
General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
Notice

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