To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
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M16C/60 Series and M16C/20 Series
General-purpose Program for Example for Initial Setting
Assembler

1. Abstract

This program is an example of initial settings accomplished by using the directive commands of the assembler.

2. Introduction

The program shown here consists of the following:

(1) Map file information output
(2) Global symbol name specification
(3) Numeric symbol definition
(4) RAM area allocation
(5) Bit symbol definition
(6) Initial setup program
  • Interrupt stack pointer setting
  • FB register setting
  • SB register setting
  • INTB register setting
  • RAM clear
(7) Main program
(8) Peripheral I/O interrupt vector table
(9) Nonmaskable interrupt fixed vector table

The following shows the range of the FB and SB relative addresses in this program.

<table>
<thead>
<tr>
<th></th>
<th>FB</th>
<th>380H to 47FH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>-128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>↑</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-400H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>↓</td>
</tr>
<tr>
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<td>+ 127</td>
</tr>
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<table>
<thead>
<tr>
<th></th>
<th>SB</th>
<th>480H to 57FH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>400H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>↓</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ 255</td>
</tr>
</tbody>
</table>
3. The example of a reference program

;******************************************************************************
; * M16C General-purpose Programs *
; CPU : M16C *
;******************************************************************************
;
; Title : Initial settings using assembler’s directive commands
;
; Outline :
; (1) Assemble control
; (2) Address control
; (3) Link control
; (4) List control
; (5) Branch instruction optimization control
;
; Notes :
;******************************************************************************
;
; Map file information output
;******************************************************************************
.
.VER 'Ver1.02' ; 'Ver1.02' is output when generating map file
;
; Global symbol name specification
;******************************************************************************
.
.GLB RUTINE ; Externally referenced symbol
.GLB MAIN ; Public symbol

.BTGLB P2_4 ; Externally referenced symbol
.BTGLB P0_7 ; Public symbol

; Numeric symbol definition
;******************************************************************************
.
VramTOP .EQU 000400H ; Declares start address of RAM
VramEND .EQU 002BFFH ; Declares last address of RAM
Vstack .EQU 002C00H ; Interrupt stack pointer
VproTOP .EQU 0F0000H ; Declares start address of program
Vintbase .EQU 0FFD00H ; Declares start address of variable vector table
Vvector .EQU 0FFFDCH ; Declares fixed interrupt vector address

CNT125ms .EQU 125 ; Sets 125 in CNT125ms
AUTOchar .EQU -8 ; Sets -8 in AUTOchar

.FORM 45,160 ; [List output control instruction]
; Specifies 45 lines, 160 columns per page of list file
.LIST ON ; [List output control]
.PAGE 'RAM' ; [List page break and title specification]
.SECTION MEMORY,DATA ; [Section name specification]
  Decls DATA attribute section of section name “MEMORY”
.ORG VramTOP ; [Absolute address setting]
  Sets location to 400H

;****************************************************************************
; RAM area allocation
;****************************************************************************
CHAR: .BLKB 10 ; [RAM area 1-byte allocation]
  Allocates 10-byte area
;
SHORT: .BLKW 10 ; [RAM area 2-byte allocation]
  Allocates 20-byte area
;
ADDR: .BLKA 10 ; [RAM area 3-byte allocation]
  Allocates 30-byte area
;
LONG: .BLKL 10 ; [RAM area 4-byte allocation]
  Allocates 40-byte area
;
SFLOAT: .BLKF 10 ; [Single-precision, floating-point RAM area allocation]
  Allocates 40-byte area
;
DFLOAT: .BLKD 10 ; [Double-precision, floating-point RAM area allocation]
  Allocates 80-byte area
;
CHECK: .BLKW 10
;
;****************************************************************************
; Bit symbol definition
;****************************************************************************
BIT4 .BTEQU 4,CHAR ; Sets bit 4 of displacement CHAR to BIT4
MSB .BTEQU 15,SHORT ; Sets bit 15 of displacement SHORT to MSB
P0_7 .BTEQU 7,3E0H ; Sets bit 7 at address 3E0 to P0_7
;
.SECTION PROG,CODE ; Declares CODE attribute section of section name “PROG”
.ORG VproTOP ; Sets location to F0000H
.OPTJ OFF ; [Branch instruction optimize specification]
  Does not optimize branch instruction after this line
.FB VramTOP ; [Assumption of FB register value]
  Assumes 400H for FB register value
.SB VramTOP+80H ; [Assumption of SB register value]
  Assumes 480H for SB register value
.FBSYM SHORT ;
.SBSYM CHECK ;
```
; Program start
;=========================================
RESET:
  LDC   #VIstack,ISP                    ; Sets interrupt stack pointer
  LDC   #VramTOP,FB                    ; Sets frame base register
  LDC   #VramTOP+80H,SB                ; Sets static base register
  LDINTB  #Vintbase                    ; Sets interrupt table register
  MOV.W  #0,R0                         ; Sets store data (0)
  MOV.W  #((VramEND+1)-VramTOP)/2,R3   ; Sets number of transfers performed
  MOV.W  #VramTOP,A1                   ; Sets address where to start storing
  SSTR.W                                      ; Executes clearing of RAM
  FSET   I                                ; Enables interrupt
;===============================================
; Main program
;===============================================
MAIN:
  MOV.W  #1234H,SHORT                   ;
  MOV.W  #5678H,CHECK                   ;
  JSR    ROUTINE                       ;(Here is your program.)
  BSET   P0_7                          
ROUTINE:                                   ;(Here is your program.)
  RTS
NOTUSE:                                    ;(Here is your program.)
  RTS
```
.PAGE     'VECTOR'
.SECTION  UINTER,ROMDATA ; Declares FOMDATA attribute section
            of section name “UINTER”
          .ORG Vintbase ; Sets location to FFD00H
;===============================================
; Peripheral I/O interrupt vector table
;===============================================
  .LWORD    NOTUSE ; Software interrupt number 0
  .LWORD    NOTUSE ; Software interrupt number 1
 .SECTION  INTER,ROMDATA ; Declares FOMDATA attribute section
            of section name “INTER”
           .ORG  Vvector ; Sets location to FFDCH
;===============================================
; Nonmaskable interrupt fixed vector table
;===============================================
  .LWORD    NOTUSE ; FFFDC to F Undefined instruction
  .LWORD    NOTUSE ; FFFE0 to 3 Overflow
  .LWORD    NOTUSE ; FFFE4 to 7 BRK instruction
  .LWORD    NOTUSE ; FFFE8 to B Address coincidence
  .LWORD    NOTUSE ; FFFEC to F Single stepping
  .LWORD    NOTUSE ; FFFFO to 3 Watchdog timer
  .LWORD    NOTUSE ; FFFF4 to 7 Debugger
  .LWORD    NOTUSE ; FFFFF to B NMI
  .LWORD    NOTUSE ; FFFFC to F Reset
;///////////////////////////////////////////////
; End of assemble direction
;///////////////////////////////////////////////
.END
;
4. Reference

SOFTWARE MANUAL
M16C/60 M16C/20 Series SOFTWARE MANUAL
(Acquire the most current version from Renesas web-site)

5. Web-site and contact for support

Renesas Web-site

http://www.renesas.com

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## REVISION HISTORY

<table>
<thead>
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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>1.00</td>
<td>Jul 08, 2002</td>
<td>- First edition issued</td>
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