To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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1. Abstract

This program adds 8 digits of BCD data together by using registers.

This program adds 8 digits of BCD data together between memory locations.

2. Introduction

This program adds 8 digits of BCD data between registers by using a decimal add instruction (DADD). Set the augend in R2 and R0 and the addend in R3 and R1 beginning with the upper half, respectively. The addition result is output to R2 and R0 beginning with the upper half. The carry information is output to the C flag.

This program adds 8 digits of BCD data between memory locations by using a decimal add instruction (DADD). Set the least significant memory address of the augend and that of the addend in the address registers. The addition result is output to the augend's memory location. The carry information is output to the C flag.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Without carry</td>
</tr>
<tr>
<td>1</td>
<td>With carry</td>
</tr>
</tbody>
</table>

### (1) BCD addition (register)

<table>
<thead>
<tr>
<th>Subroutine name</th>
<th>ROM capacity</th>
<th>Interrupt during execution</th>
<th>Number of stacks used</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCD_ADDITION8</td>
<td>13 bytes</td>
<td>Accepted</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register/memory</th>
<th>Input</th>
<th>Output</th>
<th>Usage condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>Lower half of augend</td>
<td>Lower half of addition result</td>
<td>←</td>
</tr>
<tr>
<td>R1</td>
<td>Lower half of addend</td>
<td>Does not change</td>
<td>←</td>
</tr>
<tr>
<td>R2</td>
<td>Upper half of augend</td>
<td>Upper half of addition result</td>
<td>←</td>
</tr>
<tr>
<td>R3</td>
<td>Upper half of addend</td>
<td>Does not change</td>
<td>←</td>
</tr>
<tr>
<td>A0</td>
<td>-</td>
<td>-</td>
<td>Unused</td>
</tr>
<tr>
<td>A1</td>
<td>-</td>
<td>-</td>
<td>Unused</td>
</tr>
<tr>
<td>C flag</td>
<td>-</td>
<td>Carry information</td>
<td>←</td>
</tr>
</tbody>
</table>

### Usage precautions

The augend is destroyed as a result of program execution.
(2) BCD addition (memory)

<table>
<thead>
<tr>
<th>Register/memory</th>
<th>Input</th>
<th>Output</th>
<th>Usage condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>-</td>
<td>Indeterminate</td>
<td>Used for calculation</td>
</tr>
<tr>
<td>R1</td>
<td>-</td>
<td>Indeterminate</td>
<td>Used for calculation</td>
</tr>
<tr>
<td>R2</td>
<td>-</td>
<td>-</td>
<td>Unused</td>
</tr>
<tr>
<td>R3</td>
<td>-</td>
<td>-</td>
<td>Unused</td>
</tr>
<tr>
<td>A0</td>
<td>Augend address</td>
<td>Does not change</td>
<td>←</td>
</tr>
<tr>
<td>A1</td>
<td>Addend address</td>
<td>Does not change</td>
<td>←</td>
</tr>
<tr>
<td>Memory indicated by A0</td>
<td>Augend</td>
<td>Result of addition</td>
<td>←</td>
</tr>
<tr>
<td>Memory indicated by A1</td>
<td>Addend</td>
<td>Does not change</td>
<td>←</td>
</tr>
<tr>
<td>C flag</td>
<td>-</td>
<td>Carry information</td>
<td>←</td>
</tr>
</tbody>
</table>

Usage precautions: The augend is destroyed as a result of program execution.

3. Flowchart

```
ENTER

Add low-order bits

Move added data

Add high-order bits including carry

Move added data

EXIT
```
4. The example of a reference program

;************************************************************************
; Title : Adding 8-digit BCD.
; Outline: Adds 8-digit BCD together using registers.
; Input: ------------------------------> Output:
; R0 (Lower half of augend) R0 (Lower half of addition result)
; R1 (Lower half of addend) R1 (Does not change)
; R2 (Upper half of augend) R2 (Upper half of addition result)
; R3 (Upper half of augend) R3 (Does not change)
; A0 ( ) A0 (Unused)
; A1 ( ) A1 (Unused)
; Stack amount used: None
; Notes : Result is returned by C flag
;************************************************************************

.SECTION PROGRAM,CODE
.ORG VromTOP ; ROM area

BCD_ADDITION8:
DADD.W R1,R0 ; Adds low-order bits
XCHG.W R2,R0
XCHG.W R3,R1
DADC.W R1,R0 ; Adds high-order bits
XCHG.W R2,R0
XCHG.W R3,R1
RTS

BCD_ADDITIONmemory8:
MOV.W [A0],R0
MOV.W [A1],R1
DADD.W R1,R0 ; Adds low-order bits
MOV.W R0,[A0]
MOV.W 2[A0],R0
MOV.W 2[A1],R1
DADC.W R1,R0 ; Adds high-order bits
MOV.W R0,2[A0]
RTS
.END
5. Reference

SOFTWARE MANUAL
M16C/60 M16C/20 Series SOFTWARE MANUAL
(Acquire the most current version from Renesas web-site)

6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com

Contact for Renesas technical support

Mail to: support_apl@renesas.com
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jul 08, 2002</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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