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Renesas Electronics Corporation

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M16C/62P and M16C/63, 64, 64A, 65 Groups
Differences in Flash Memory CPU Rewrite Modes

1. Abstract

This document describes differences in flash memory CPU rewrite modes between the M16C/62P Group and M16C/63, 64, 64A and 65 Groups.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/62P Group
  - M16C/63 Group
  - M16C/64 Group
  - M16C/64A Group
  - M16C/65 Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the hardware manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Specification Comparison

Table 3.1 lists the differences in the flash memory CPU rewrite modes.

<table>
<thead>
<tr>
<th>Item</th>
<th>M16C/62P Group</th>
<th>M16C/63, 64, 64A and 65 Groups</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash-related registers</td>
<td>FIDR, FMR0, FMR1</td>
<td>FMR0, FMR1, FMR2, FMR3 (M16C/63 only), FMR6, and PRG2C</td>
</tr>
<tr>
<td>Flash areas</td>
<td>User ROM</td>
<td>Program ROM 1</td>
</tr>
<tr>
<td></td>
<td>Data flash (block A)</td>
<td>Program ROM 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data flash (block A, block B)</td>
</tr>
<tr>
<td>Registers used and settings in EW0 mode</td>
<td>FMR0 bit (^{1}) is 1</td>
<td>FMR01 bit (^{1}) is 1</td>
</tr>
<tr>
<td></td>
<td>FMR11 bit (^{2}) is 0</td>
<td>FMR11 bit (^{2}) is 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FMR6 register is 02h</td>
</tr>
<tr>
<td>Registers used and settings in EW1 mode</td>
<td>FMR01 bit (^{1}) is 1</td>
<td>FMR01 bit (^{1}) is 1</td>
</tr>
<tr>
<td></td>
<td>FMR11 bit (^{2}) is 1</td>
<td>FMR11 bit (^{2}) is 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FMR6 register is 03h</td>
</tr>
<tr>
<td>Software commands</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program</td>
<td>In 1-word (2-byte) units</td>
<td>In 2-word (4-byte) units</td>
</tr>
<tr>
<td>Command code</td>
<td>xx40h</td>
<td>xx41h</td>
</tr>
<tr>
<td>Erase all unlocked block</td>
<td>Yes</td>
<td>N/A</td>
</tr>
<tr>
<td>Block blank check</td>
<td>N/A</td>
<td>Yes (FMR05 bit is 1)</td>
</tr>
<tr>
<td>User boot function</td>
<td>N/A</td>
<td>Yes: M16C/63</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A: M16C/64, 64A, 65</td>
</tr>
</tbody>
</table>

Notes:
1. The FMR01 bit is bit 1 in the FMR0 register.
2. The FMR11 bit is bit 1 in the FMR1 register.
4. Detailed Comparison

4.1 Flash-related Register Comparison

Table 4.1 lists the differences in the flash memory CPU rewrite modes.

<table>
<thead>
<tr>
<th>Item</th>
<th>M16C/62P Group</th>
<th>M16C/63, 64, 64A and 65 Groups</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash Memory Control Register 0 (FMR0)</td>
<td>User ROM area select bit (1) 0: Boot ROM area is accessed 1: User ROM area is accessed</td>
<td>Reserved bit Set to 0 when not in user boot mode. Set to 1 in user boot mode.</td>
</tr>
<tr>
<td>Flash Memory Control Register 1 (FMR1)</td>
<td>EW1 mode select bit 0: EW0 mode 1: EW1 mode</td>
<td>Write to FMR6 register enable bit register 0: Disabled 1: Enabled</td>
</tr>
<tr>
<td>Flash Memory Control Register 2 (FMR2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash Memory Control Register 6 (FMR6)</td>
<td>EW1 mode select bit 0: EW0 mode 1: EW1 mode</td>
<td></td>
</tr>
<tr>
<td>Program 2 Area Control Register (PRG2C)</td>
<td>Program ROM 2 disable bit 0: Enable program ROM 2 1: Disable program ROM 2</td>
<td>Program ROM 1 of addresses (40000h to 7FFFFh) (2) 0: Disabled 1: Enabled</td>
</tr>
</tbody>
</table>

Notes:
1. Only applies when in boot mode.
2. In the M16C/65 Group, only in products with program ROM 1 over 512 KB.
4.2 Memory Map of Flash Memory Area

The memory map of flash memory and its block size differ between the M16C/62P Group and the M16C/63, 64, 64A and 65 Groups.

Table 4.2 lists the differences in memory maps of their flash area. Figure 4.1 shows the comparison of memory maps.

<table>
<thead>
<tr>
<th>Item</th>
<th>M16C/62P Group</th>
<th>M16C/63, 64, 64A and 65 Groups</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data flash</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block A (4 KB)</td>
<td>0F000h to 0FFFFh</td>
<td>0E000h to 0EFFFh</td>
</tr>
<tr>
<td>Block B (4 KB)</td>
<td>N/A</td>
<td>0F000h to 0FFFFh</td>
</tr>
<tr>
<td>Program ROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program ROM 1</td>
<td>080000h to 0FFFFFh (2)</td>
<td>080000h to 0FFFFFh (2)</td>
</tr>
<tr>
<td>Program ROM 2</td>
<td>N/A</td>
<td>010000h to 013FFFh (3)</td>
</tr>
</tbody>
</table>

Notes:
2. Applies to the 512 KB version.
3. Can be used when the PRG2C0 bit in the PRG2C register is 0 (enable program ROM 2).
### Figure 4.1 Comparison of Memory Maps (512 KB Version)

#### M16C/62P Group

<table>
<thead>
<tr>
<th>Block</th>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>00E000h - 00EFFFh</td>
</tr>
<tr>
<td></td>
<td>Block A: 4 KB</td>
</tr>
<tr>
<td>0</td>
<td>0F0000h - 0F0FFFh</td>
</tr>
<tr>
<td></td>
<td>Block F: 4 KB</td>
</tr>
</tbody>
</table>

#### M16C/63, 64, 64A, and 65 Groups

<table>
<thead>
<tr>
<th>Block</th>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00E000h - 00EFFFh</td>
</tr>
<tr>
<td></td>
<td>Block A: 4 KB</td>
</tr>
<tr>
<td>0</td>
<td>00F000h - 00FFFFh</td>
</tr>
<tr>
<td></td>
<td>Block B: 4 KB</td>
</tr>
<tr>
<td>0</td>
<td>010000h - 013FFFh</td>
</tr>
<tr>
<td></td>
<td>Program ROM 2: 16 KB</td>
</tr>
<tr>
<td>0</td>
<td>013FFFh</td>
</tr>
</tbody>
</table>

#### Differences in Flash Memory CPU Rewrite Modes

- **Program ROM 1**
  - Block 1: 4 KB
  - Block 2: 8 KB
  - Block 3: 8 KB
  - Block 4: 32 KB

- **Program ROM 2**
  - Block 5: 64 KB
  - Block 6: 64 KB
  - Block 7: 64 KB
  - Block 8: 64 KB

- **Data Flash**
  - Block 9: 64 KB
  - Block 10: 64 KB
  - Block 11: 64 KB
  - Block 12: 64 KB
4.3 Setting and Resetting of CPU Rewrite Mode (EW0, EW1 Mode)

Figure 4.2 shows the Comparison of Setting and Resetting of CPU Rewrite Mode (EW0 Mode). Figure 4.3 shows the Comparison of Setting and Resetting of CPU Rewrite Mode (EW1 Mode).

---

### Figure 4.2 Comparison of Setting and Resetting of CPU Rewrite Mode (EW0 Mode)

#### M16C/62P Group

1. **Single-chip mode, memory expansion mode or boot mode**
2. **Transfer the rewrite control program to the areas other than flash memory.**
3. **Set registers CM0, CM1 and PM1.**
4. **Jump to the rewrite control program transferred to an area other than the flash memory.**

#### Rewrite control program

- **In boot mode only**
  - Set the FMR05 bit to 1 (user ROM area accessed).
- **Write 0 and then 1 to the FMR01 bit (CPU rewrite mode enabled).**
- **Execute the software commands.**
- **Execute the read array command.**
- **Set the FMR01 bit to 0 (CPU rewrite mode disabled).**
- **In boot mode only**
  - Set the FMR05 bit to 1 (user ROM area accessed).**
- **Jump to the desired address in the flash memory.**

#### Notes:

1. In CPU rewrite mode, set the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to CPU clock frequency of 10.0 MHz or less. Set the PM17 bit in the PM1 register to 1 (wait inserted).
2. Set the FMR01 bit to 1 immediately after setting it to 0. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1.
3. Exit CPU rewrite mode after executing the read array command.
4. When CPU rewrite mode is exited while FMR05 bit is set to 1, the user ROM area can be accessed.
5. When in CPU rewrite mode, bits PM10 and PM13 in the PM1 register are set to 1. The rewrite control program can only be executed in the internal RAM or in an external area that is enabled for use when the PM13 bit = 1. When the PM13 bit = 0 and the flash memory is used in 4M-byte mode, the extended accessible area (40000h to BFFFFh) cannot be used.

---

### Figure 4.3 Comparison of Setting and Resetting of CPU Rewrite Mode (EW1 Mode)

#### M16C/63, 64, 64A and 65 Groups

1. **Single-chip mode or memory expansion mode**
2. **Transfer the rewrite control program to the areas other than flash memory.**
3. **Set registers CM0, CM1 and PM1.**
4. **Jump to the rewrite control program transferred to an area other than the flash memory.**

#### Rewrite control program

- **In boot mode only**
  - Set the FMR05 bit to 1 (user ROM area accessed).
- **Write 0 and then 1 to the FMR01 bit (CPU rewrite mode enabled).**
- **Set the FMR11 bit to 1 (FMR6 register write enabled), then set the FMR6 register to 02h (EW0 mode), and then set the FMR11 bit to 0 (FMR6 register write disabled).**
- **Execute the software commands.**
- **Execute the read array command.**
- **Set the FMR01 bit to 0 (CPU rewrite mode disabled).**
- **In boot mode only**
  - Set the FMR05 bit to 1 (user ROM area accessed).**
- **Jump to the desired address in the flash memory.**

#### Notes:

1. In CPU rewrite mode, set the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to CPU clock frequency of 10.0 MHz or less. Set the PM17 bit in the PM1 register to 1 (with wait inserted).
2. Set the FMR01 bit to 1 immediately after setting it to 0. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1.
3. Exit CPU rewrite mode after executing the read array command.
4. When in CPU rewrite mode, bits PM10 and PM13 in the PM1 register are set to 1. The rewrite control program can only be executed in the internal RAM or in an external area which can be used when both bits PM10 and PM13 are 1. When the PM13 bit = 0 and the flash memory is used in 4-MB mode, the extended accessible area (40000h to BFFFFh) cannot be used.
M16C/62P and M16C/63, 64, 64A, 65 Groups

Differences in Flash Memory CPU Rewrite Modes

Figure 4.3 Comparison of Setting and Resetting of CPU Rewrite Mode (EW1 Mode)

### M16C/62P Group

1. **Single-chip mode**

2. Set the CM0, CM1 and PM1 registers. \(^{(1)}\)

3. Set the FMR01 bit to 1 (CPU rewrite mode enabled) after writing 0.

4. Set the FMR11 bit to 1 (EW1 mode) after writing 0. \(^{(2)}\)

5. Execute the software commands.

6. Set the FMR01 bit to 0 (CPU rewrite mode disabled).

### M16C/63, 64, 64A and 65 Groups

1. **Single-chip mode**

2. Set the CM0, CM1 and PM1 registers. \(^{(1)}\)

3. Set the FMR01 bit to 1 (CPU rewrite mode enabled) after writing 0.

4. Set the FMR11 bit to 1 (FMR6 register write enabled), then set the FMR6 register to 03h (EW0 mode), and then set the FMR11 bit to 0 (FMR6 register write disabled).

5. Execute the software commands.

6. Set the FMR01 bit to 0 (CPU rewrite mode disabled).

### Notes:

1. In EW1 mode, do not enter memory expansion or boot mode.
2. In CPU rewrite mode, set the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to CPU clock frequency of 10.0 MHz or less. Set the PM17 bit in the PM1 register to 1 (wait inserted).
3. Set the FMR01 bit to 1 immediately after setting it to 0.
   Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1.
   Set the FMR11 bit to 1 immediately after setting it to 0 while the FMR01 bit is set to 1.
   Do not generate an interrupt or a DMA transfer between setting the FMR11 bit to 0 and setting it to 1.
   Set bits FMR01 and FMR11 while “H” is applied to the NMI pin.
4. In EW1 mode, do not enter memory expansion or boot mode.
5. In CPU rewrite mode, set the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to CPU clock frequency of 10.0 MHz or less. Set the PM17 bit in the PM1 register to 1 (wait inserted).
6. Set the FMR01 bit to 1 immediately after setting it to 0.
   Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1.
   Set the FMR11 bit to 1 when the FMR01 bit is set to 1.
### 4.4 Operation Example

Table 4.3 lists the differences in the software commands.

#### Table 4.3 Differences in Software Commands

<table>
<thead>
<tr>
<th>Software Command</th>
<th>MCU</th>
<th>The First Bus Cycle</th>
<th>The Second Bus Cycle</th>
<th>The Third Bus Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Address</td>
<td>Data</td>
<td>Address</td>
</tr>
<tr>
<td>Read array</td>
<td>M16C/62P</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>B0-7</td>
<td>xxFFh</td>
<td>B8</td>
</tr>
<tr>
<td>Read status register</td>
<td>M16C/62P</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>BA</td>
<td>xxFFh</td>
<td>B8</td>
</tr>
<tr>
<td>Clear status register</td>
<td>M16C/62P</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xxFFh</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>BA</td>
<td>xxFFh</td>
<td>B8</td>
</tr>
<tr>
<td>Program</td>
<td>M16C/62P</td>
<td>WA</td>
<td>xx40h</td>
<td>WA</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>WA</td>
<td>xx41h</td>
<td>WA</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>WA</td>
<td>xx41h</td>
<td>WA</td>
</tr>
<tr>
<td>Block erase</td>
<td>M16C/62P</td>
<td>x</td>
<td>xx20h</td>
<td>BA</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xx20h</td>
<td>BA</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>BA</td>
<td>xx20h</td>
<td>BA</td>
</tr>
<tr>
<td>Erase all unlocked block</td>
<td>M16C/62P</td>
<td>x</td>
<td>xxA7h</td>
<td>x</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Read lock bit status</td>
<td>M16C/62P</td>
<td>x</td>
<td>xx71h</td>
<td>BA</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xx71h</td>
<td>BA</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>BA</td>
<td>xx71h</td>
<td>BA</td>
</tr>
<tr>
<td>Block blank check</td>
<td>M16C/62P</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>M16C/63, 64, 64A, 65 (1)</td>
<td>x</td>
<td>xx25h</td>
<td>BA</td>
</tr>
<tr>
<td></td>
<td>M16C/65 (2)</td>
<td>BA</td>
<td>xx25h</td>
<td>BA</td>
</tr>
</tbody>
</table>

**Notes:**
1. In the M16C/65 Group, only in products with program ROM 1 that is 512 KB or less.
2. In the M16C/65 Group, only in products with program ROM 1 over 512 KB.
SRD: Status register data (D7 to D0)
WA: Write address (Even address. Set the end of the address to 0h, 4h, 8h, or Ch in the M16C/63, 64, 64A and 65 Groups).
WD: Write data (16 bits).
WD0: Write data low-order word (16 bits).
WD1: Write data high-order word (16 bits).
BA: Highest-order block address (even address)
B0-7: Any even address in blocks 0 to 7, program ROM 2, or data flash
B8: Any even address in blocks after 8.
x: Any even address in user ROM area
xx: Eight high-order bits of command code (ignored)
4.5 Program
The program differs between the M16C/62P Group and the M16C/63, 64, 64A and 65 Groups. Table 4.4 lists the differences in the programs.

Table 4.4 Differences in programs

<table>
<thead>
<tr>
<th>Item</th>
<th>M16C/62P Group</th>
<th>M16C/63, M16C/64, M16C/64A and M16C/65 Groups</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write unit</td>
<td>In 1-word (2-byte) units</td>
<td>In 2-word (4-byte) units</td>
</tr>
<tr>
<td>Command code</td>
<td>xx40h</td>
<td>xx41h</td>
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</table>

4.6 User Boot Function
In the M16C/63, 64, 64A and 65 Groups, user boot functions is added to select boot mode and user boot mode by the status of a port. Refer to each device's hardware manual for details on the boot function.

4.7 Suspend Function
The M16C/63 Group includes a suspend function for suspending automatic programming and erasure. Refer to the M16C/63 Group hardware manual for details.
5. Reference Documents

Hardware Manuals
M16C/62P Group Hardware Manual
M16C/63 Group Hardware Manual
M16C/64 Group Hardware Manual
M16C/64A Group Hardware Manual
M16C/65 Group Hardware Manual
The latest versions can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.
### REVISION HISTORY

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